

# NT7107D

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## INTRODUCTION

The NT7107 is a LCD driver LSI with 64 channel outputs for dot matrix liquid crystal graphic display systems. This device provides 64 shift registers and 64 output drivers. It generates the timing signal to control the NT7108.

The NT7107 is fabricated by low power CMOS high voltage process technology, and is composed of the liquid crystal display system in combination with the NT7108 (64 channel segment driver).

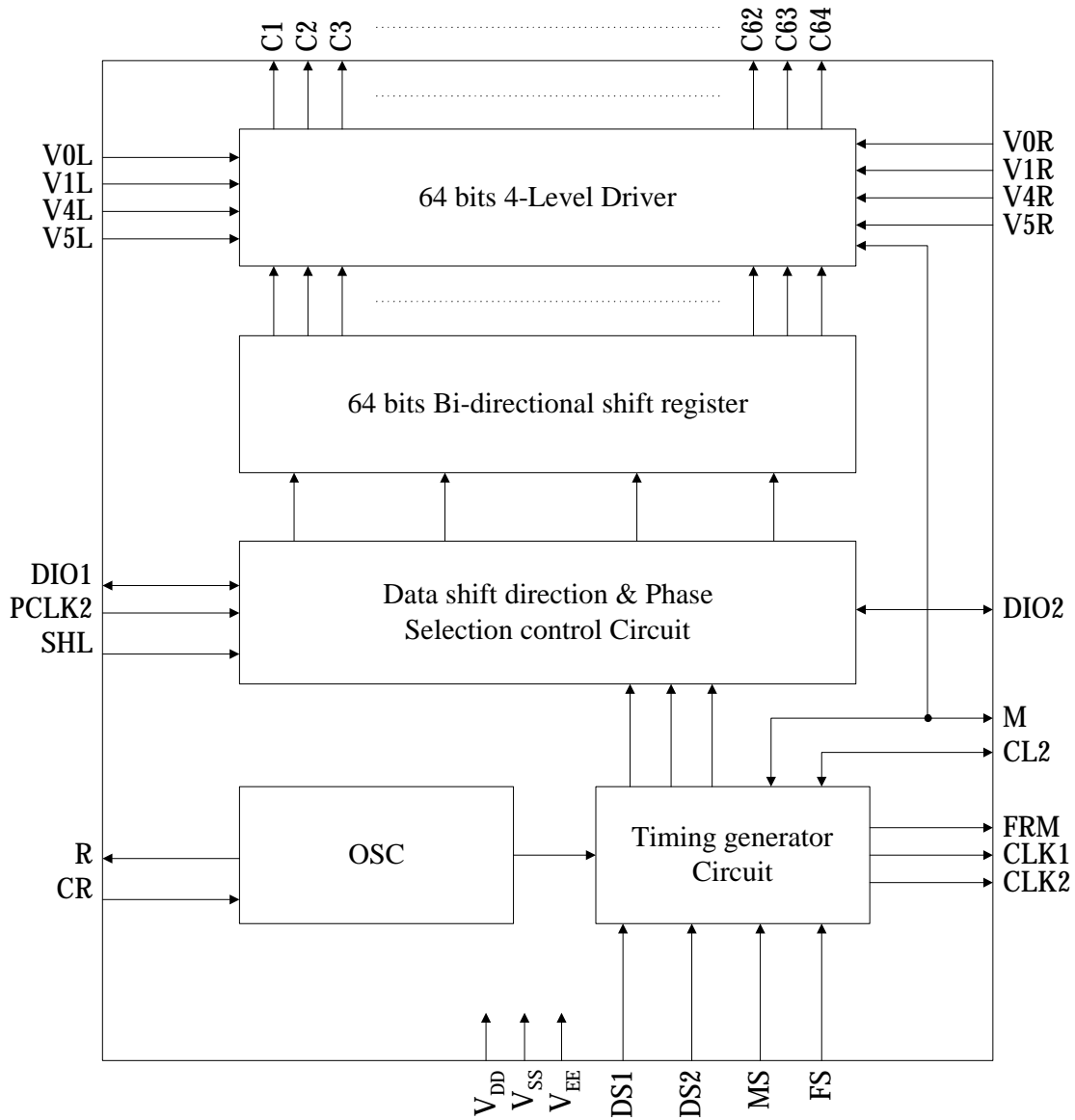
## FEATURES

- Dot matrix LCD common driver with 64 channel output
- 64-bit shift register at internal LCD driver circuit
- Internal timing generator circuit for dynamic display
- Selection of master/slave mode
- Applicable LCD duty: 1/48, 1/64, 1/96, 1/128
- Power supply voltage: +2.7~+5.5V
- LCD driving voltage: 8V~17V ( $V_{DD}-V_{EE}$ )
- Interface

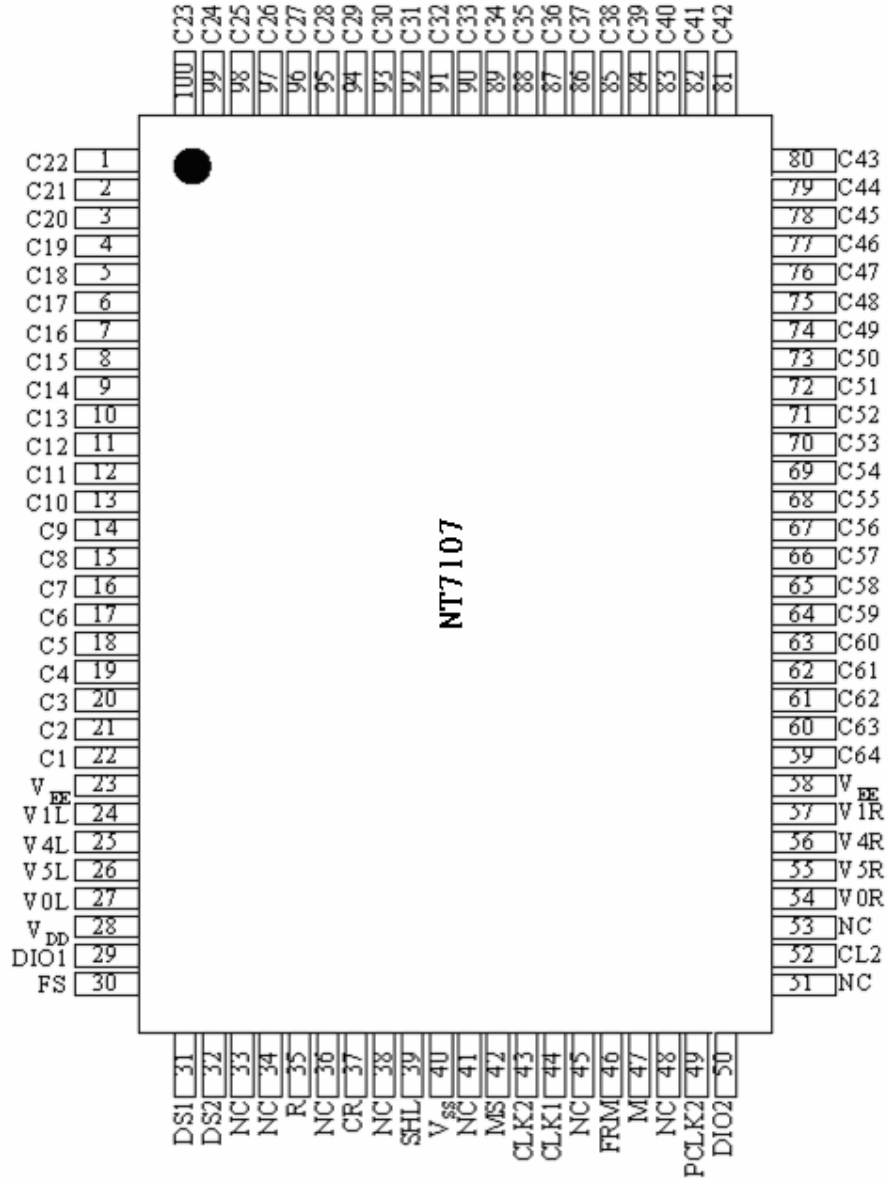
Driver		Controller
COMMON	SEGMENT	
Other NT7107	Other NT7108	MPU

- High voltage CMOS process
- Bare chip, QFP 100L, LQFP 100L available

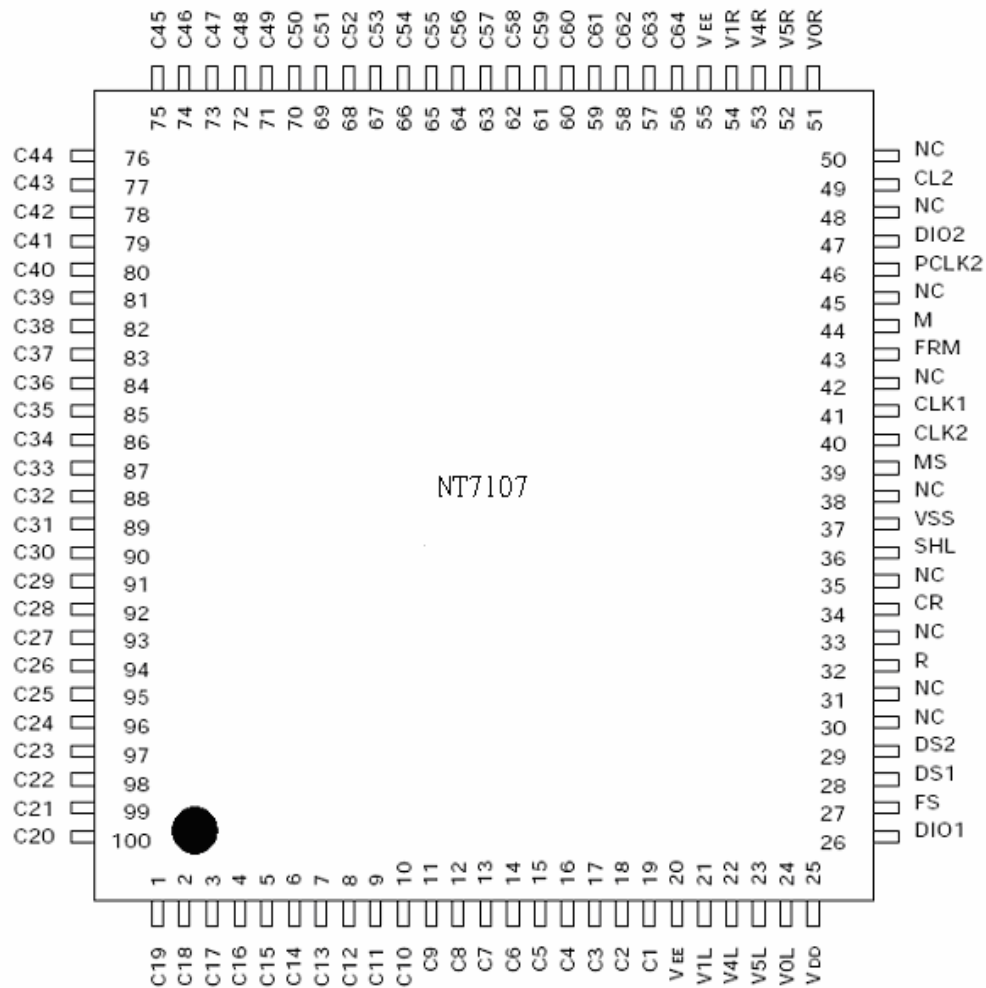
**BLOCK DIAGRAM**



**PIN CONFIGURATION**  
**QFP 100L PACKAGE**

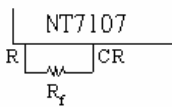
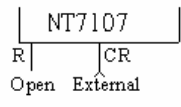
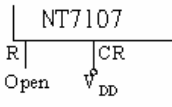


**LQFP 100L PACKAGE**



**PIN DESCRIPTION**
**Table 1. Pin Description**

Symbol	I/O	Description													
V <sub>DD</sub>	Power	For internal logic circuit (+2.7~+5.5V)													
V <sub>SS</sub>		GND (=0V)													
V <sub>EE</sub>		For LCD driver circuit													
V <sub>0L</sub> , V <sub>0R</sub>	Power	Bias supply voltage terminals to drive LCD. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Select Level</th> <th>Non-Select Level</th> </tr> </thead> <tbody> <tr> <td>V<sub>0L</sub> (R), V<sub>5L</sub> (R)</td> <td>V<sub>1L</sub> (R), V<sub>4L</sub> (R)</td> </tr> </tbody> </table>	Select Level	Non-Select Level	V <sub>0L</sub> (R), V <sub>5L</sub> (R)	V <sub>1L</sub> (R), V <sub>4L</sub> (R)									
Select Level			Non-Select Level												
V <sub>0L</sub> (R), V <sub>5L</sub> (R)			V <sub>1L</sub> (R), V <sub>4L</sub> (R)												
V <sub>1L</sub> , V <sub>1R</sub>															
V <sub>4L</sub> , V <sub>4R</sub>															
V <sub>5L</sub> , V <sub>5R</sub>															
	The same voltage should connect V <sub>0L</sub> and V <sub>0R</sub> (V <sub>1L</sub> & V <sub>1R</sub> , V <sub>4L</sub> & V <sub>4R</sub> , V <sub>5L</sub> & V <sub>5R</sub> ).														
MS	Input	Section of master/slave mode <ul style="list-style-type: none"> <li>· Master mode (MS=1) DIO1, DIO2, CL2 and M is output state.</li> <li>· Slave mode (MS=0) SHL=1 DIO1 is input state (DIO2 is output state) SHL=0 DIO2 is input state (DIO1 is output state) CL2 and M are input state.</li> </ul>													
SHL	Input	Selection of data shift direction. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>SHL</th> <th>Data Shift Direction</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>DIO1 C1...C64 DIO2</td> </tr> <tr> <td>L</td> <td>DIO2 C64...C1 DIO1</td> </tr> </tbody> </table>	SHL	Data Shift Direction	H	DIO1 C1...C64 DIO2	L	DIO2 C64...C1 DIO1							
SHL	Data Shift Direction														
H	DIO1 C1...C64 DIO2														
L	DIO2 C64...C1 DIO1														
PCLK2	Input	Selection of shift clock (CL2) phase. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>PCLK2</th> <th>Data Clock (CL2) Phase</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>Data shift at the rising edge of CL2</td> </tr> <tr> <td>L</td> <td>Data shift at the falling edge of CL2</td> </tr> </tbody> </table>	PCLK2	Data Clock (CL2) Phase	H	Data shift at the rising edge of CL2	L	Data shift at the falling edge of CL2							
PCLK2	Data Clock (CL2) Phase														
H	Data shift at the rising edge of CL2														
L	Data shift at the falling edge of CL2														
FS	Input	Selection of oscillation frequency. <ul style="list-style-type: none"> <li>· Master mode when the frame frequency is 70 Hz, the oscillation frequency should be fosc=430kHz at FS=1(V<sub>DD</sub>) fosc=215kHz at FS=0(V<sub>SS</sub>)</li> <li>· Slave mode Connect to V<sub>DD</sub></li> </ul>													
DS1 DS2	Input	Selection of display duty. <ul style="list-style-type: none"> <li>· Master mode  <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>DS1</th> <th>DS2</th> <th>Duty</th> </tr> </thead> <tbody> <tr> <td rowspan="2">L</td> <td>L</td> <td>1/48</td> </tr> <tr> <td>H</td> <td>1/64</td> </tr> <tr> <td rowspan="2">H</td> <td>L</td> <td>1/96</td> </tr> <tr> <td>H</td> <td>1/128</td> </tr> </tbody> </table> </li> <li>· Slave mode: Connect to V<sub>DD</sub>.</li> </ul>	DS1	DS2	Duty	L	L	1/48	H	1/64	H	L	1/96	H	1/128
DS1	DS2	Duty													
L	L	1/48													
	H	1/64													
H	L	1/96													
	H	1/128													

Symbol	I/O	Description																		
R CR		RC Oscillator (Built-in capacitor) <ul style="list-style-type: none"> <li>Master mode: Use these terminals as shown below.</li> </ul>   <ul style="list-style-type: none"> <li>Slave mode: Stop the oscillator as shown below.</li> </ul> 																		
CLK1 CLK2	Output	Operating clock output for the NT7108 <ul style="list-style-type: none"> <li>Master mode: connection to CLK1 and CLK2 of the NT7108</li> <li>Slave mode: open</li> </ul>																		
FRM	Output	Synchronous frame signal. <ul style="list-style-type: none"> <li>Master mode: connection to FRM of the NT7108</li> <li>Slave mode: open</li> </ul>																		
M	Input/ Output	Alternating signal input for LCD driving. <ul style="list-style-type: none"> <li>Master mode: output state Connection to M of the NT7108</li> <li>Slave mode: input state Connection to the controller</li> </ul>																		
CL2	Input/ Output	Data shift clock <ul style="list-style-type: none"> <li>Master mode: output state Connection to CL of the NT7108</li> <li>Slave mode: input state connection to shift clock terminal of the controller.</li> </ul>																		
DIO1 DIO2	Input/ Output	Data input/output pins of internal shift register. <table border="1" data-bbox="467 1129 1104 1312"> <thead> <tr> <th>MS</th> <th>SHL</th> <th>DIO1</th> <th>DIO2</th> </tr> </thead> <tbody> <tr> <td rowspan="2">H</td> <td>H</td> <td>Output</td> <td>Output</td> </tr> <tr> <td>L</td> <td>Output</td> <td>Output</td> </tr> <tr> <td rowspan="2">L</td> <td>H</td> <td>Input</td> <td>Output</td> </tr> <tr> <td>L</td> <td>Output</td> <td>Input</td> </tr> </tbody> </table>	MS	SHL	DIO1	DIO2	H	H	Output	Output	L	Output	Output	L	H	Input	Output	L	Output	Input
MS	SHL	DIO1	DIO2																	
H	H	Output	Output																	
	L	Output	Output																	
L	H	Input	Output																	
	L	Output	Input																	
C1-C64	Output	Common signal output for LCD driving. <table border="1" data-bbox="467 1375 1031 1558"> <thead> <tr> <th>Data</th> <th>M</th> <th>Out</th> </tr> </thead> <tbody> <tr> <td rowspan="2">L</td> <td>L</td> <td>V1</td> </tr> <tr> <td>H</td> <td>V4</td> </tr> <tr> <td rowspan="2">H</td> <td>L</td> <td>V5</td> </tr> <tr> <td>H</td> <td>V0</td> </tr> </tbody> </table>	Data	M	Out	L	L	V1	H	V4	H	L	V5	H	V0					
Data	M	Out																		
L	L	V1																		
	H	V4																		
H	L	V5																		
	H	V0																		
NC		No connection																		

**MAXIMUM ABSOLUTE LIMIT**

Characteristic	Symbol	Value	Unit	Note
Operating voltage	$V_{DD}$	-0.3 to +7.0	V	(1)
Supply voltage	$V_{EE}$	$V_{DD}-19.0$ to $V_{DD}+0.3$		(4)
Driver supply voltage	$V_B$	-0.3 to $V_{DD}+0.3$		(1),(2)
	$V_{LCD}$	$V_{EE}-0.3$ to $V_{DD}+0.3$		(3),(4)
Operating temperature	$T_{OPR}$	-30 to +85	°C	-
Storage temperature	$T_{STG}$	-55 to +125		-

**NOTES:**

1. Based on  $V_{SS}=0V$
2. Applies to input terminals and I/O terminals at high impedance. (Except  $V_{0L(R)}$ ,  $V_{1L(R)}$ ,  $V_{4L(R)}$  and  $V_{5L(R)}$ )
3. Applies to  $V_{0L(R)}$ ,  $V_{1L(R)}$ ,  $V_{4L(R)}$  and  $V_{5L(R)}$ .
4. Voltage level:  $V_{DD} \geq V_{0L}=V_{0R} \geq V_{1L}=V_{1R} \geq V_{4L}=V_{4R} \geq V_{5L}=V_{5R} \geq V_{EE}$ .

**ELECTRICAL CHARACTERISTICS**
**DC CHARACTERISTICS** ( $V_{DD}=+5.0V$ ,  $V_{SS}=0V$ ,  $|V_{DD}-V_{EE}|=8\sim 17V$ ,  $T_A=-30 \sim +85^\circ C$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating voltage	$V_{DD}$	-	2.7	-	5.5	V	(1)
Input Voltage	High $V_{IH}$	-	$0.7V_{DD}$	-	$V_{DD}$		
	Low $V_{IL}$	-	$V_{SS}$	-	$0.3V_{DD}$		
Output Voltage	High $V_{OH}$	$I_{OH}=-0.4mA$	$V_{DD}-0.4$	-	-		
	Low $V_{OL}$	$I_{OL}=0.4mA$	-	-	0.4		
Input leakage current	$I_{LKG}$	$V_{IN}=V_{DD}-V_{SS}$	-1.0	-	1.0	$\mu A$	(1)
OSC frequency	$f_{OSC}$	$R_f=47K\Omega \pm 2\%$	315	450	585	kHz	
On resistance ( $V_{DIV} - C_i$ )	$R_{ON}$	$V_{DD}-V_{EE}=17V$ Load current = $\pm 150\mu A$	-	-	1.5	K $\Omega$	
Operating current	$I_{DD1}$	Master mode; 1/128duty	-	-	1.0	mA	
	$I_{DD2}$	Slave mode; 1/128 duty	-	-	200	$\mu A$	(4)
Supply current	$I_{EE}$	Master mode; 1/128 duty	-	-	100		(5)
Operating Frequency	$f_{OP1}$	Master mode; External clock	50	-	600	kHz	
	$f_{OP2}$	Slave mode	0.5	-	1500		

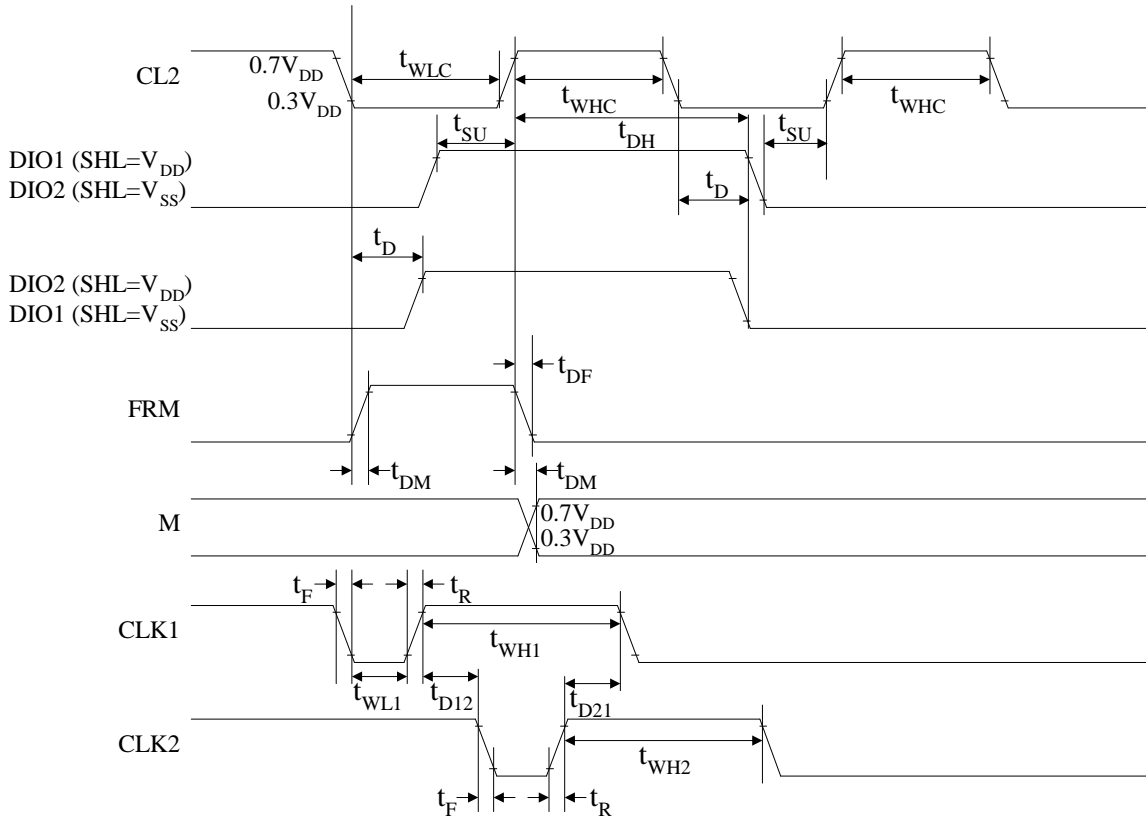
**NOTES:**

1. Applies to input terminals FS, DS1, DS2, CR, SHL, MS and PCLK2 and I/O terminals DIO1, DIO2, M and CL2 in the input state.
2. Applies to output terminals CLK1, CLK2 and FRM and I/O terminals DIO1, DIO2, M and CL2 in the Output State.
3. This value is specified at about the current flowing through  $V_{SS}$ . Internal oscillation circuit:  $R_f = 47k\Omega$ , Each terminal of DS1, DS2, FS, SHL and MS is connected to  $V_{DD}$  and out is no load.
4. This value is specified at about the current flowing through  $V_{SS}$ . Each terminal of DS1, DS2, FS, SHL, PCLK2 and CR is connected to  $V_{DD}$ , and MS is connected to  $V_{SS}$ . CL2, M, DIO1 is external clock.
5. This value is specified at the current flowing through  $V_{EE}$ . Don't connect to  $V_{LCD}$  (V1-V5).



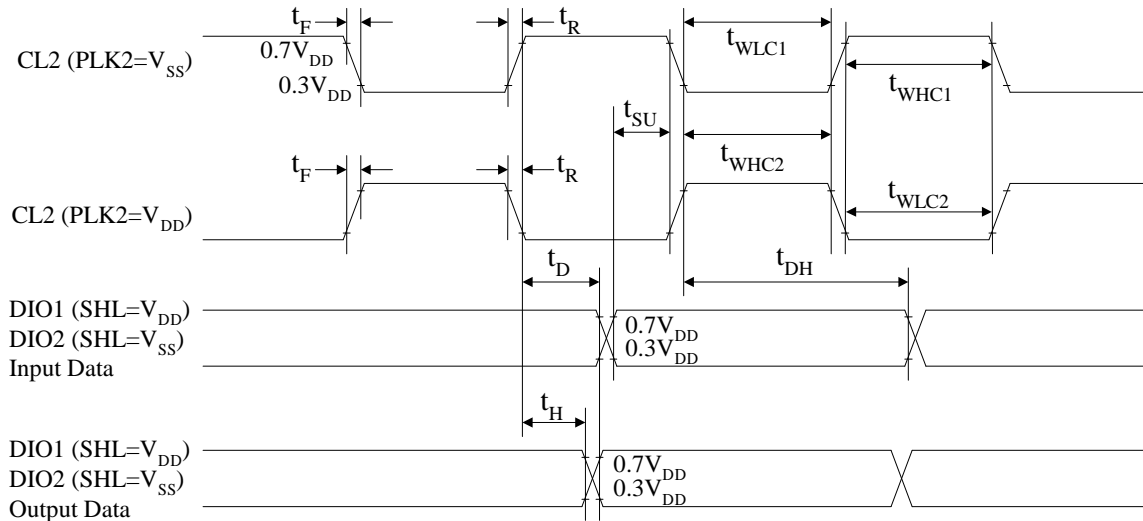
**AC CHARACTERISTICS ( $V_{DD}=5V\pm 10\%$ ,  $T_A=-30\sim+85^\circ C$ )**

**Master Mode ( $MS=V_{DD}$ ,  $PCLK2=V_{DD}$ )**



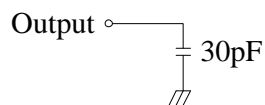
**Master Mode**

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Data setup time	$t_{SU}$	20	-	-	$\mu s$
Data hold time	$t_{DH}$	40	-	-	
Data delay time	$t_D$	5	-	-	
FRM delay time	$t_{DF}$	-2	-	2	
M delay time	$t_{DM}$	-2	-	2	
CL2 low level width	$t_{WLC}$	35	-	-	
CL2 high level width	$t_{WHC}$	35	-	-	ns
CLK1 low level width	$t_{WL1}$	700	-	-	
CLK2 low level width	$t_{WL2}$	700	-	-	
CLK1 high level width	$t_{WH1}$	2100	-	-	
CLK2 high level width	$t_{WH2}$	2100	-	-	
CLK1-CLK2 phase difference	$t_{D12}$	700	-	-	
CLK2-CLK1 phase difference	$t_{D21}$	700	-	-	
CLK1,CLK2 rise/fall time	$t_R/ t_F$	-	-	150	

**Slave Mode (MS=V<sub>SS</sub>)**


Characteristic	Symbol	Min.	Typ.	Max.	Unit	Note
CL2 low level width	t <sub>WLC1</sub>	450	-	-	ns	PCLK2=V <sub>SS</sub>
CL2 high level width	t <sub>WHC1</sub>	150	-	-		PCLK2=V <sub>SS</sub>
CL2 low level width	t <sub>WLC2</sub>	150	-	-		PCLK2=V <sub>DD</sub>
CL2 high level width	t <sub>WHC2</sub>	450	-	-		PCLK2=V <sub>DD</sub>
Data setup time	t <sub>SU</sub>	100	-	-		
Data hold time	t <sub>DH</sub>	100	-	-		
Data delay time	t <sub>D</sub>	-	-	200		(NOTE)
Output data hold time	t <sub>H</sub>	10	-	-		
CL2 rise/fall time	t <sub>R</sub> / t <sub>F</sub>	-	-	30		

**NOTE:** Connect load CL = 30pF

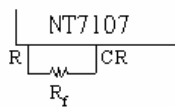


## FUNCTIONAL DESCRIPTION

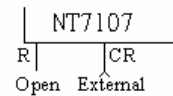
### RC Oscillator

The RC Oscillator generates CL2, M, FRM of the NT7107, and CLK1 and CLK1 of the NT7108 by the oscillation resistor R and internal capacitor C. When selecting the master/slave mode, the oscillation circuit is as following:

Master Mode: In the master mode, use these terminals as shown below.

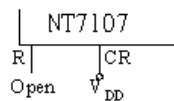


Internal Oscillation( $R_f=47k\Omega$ )



External Clock

Slave Mode: In the slave mode, stop the oscillator as shown below.



### Timing Generation Circuit

It generates CL2, M, FRM, CLK1 and CLK2 by the frequency from the oscillation circuit.

Selection of Master/Slave (M/S) Mode

When MS is H, it generates CL2, M, FRM, CLK1 and CLK2 internally.

When MS is L, it operates by receiving M and CL2 from the master device.

Frequency Selection (FS)

To adjust FRM frequency by 70Hz, the oscillation frequency should be as follows:

FS	Oscillation Frequency
H	$f_{OSC}=430kHz$
L	$f_{OSC}=215kHz$

In the slave mode, it is connected to  $V_{DD}$ .

### Duty Selection (DS1, DS2)

It provides various duty selections according to DS1 and DS2.

DS1	DS2	Duty
L	L	1/48
	H	1/64
H	L	1/96
	H	1/128

**Data Shift & Phase Select Control**

## Phase Selection

It is a circuit to shift data on synchronization of rising edge, or falling edge of the CL2 according to PCLK2.

<b>PCLK2</b>	<b>Phase Selection</b>
H	Data shift on rising edge of CL2
L	Data shift on falling edge of CL2

## Data shift Direction Selection

When MS is connected to V<sub>DD</sub>, DIO1 and DIO2 terminal is only output.

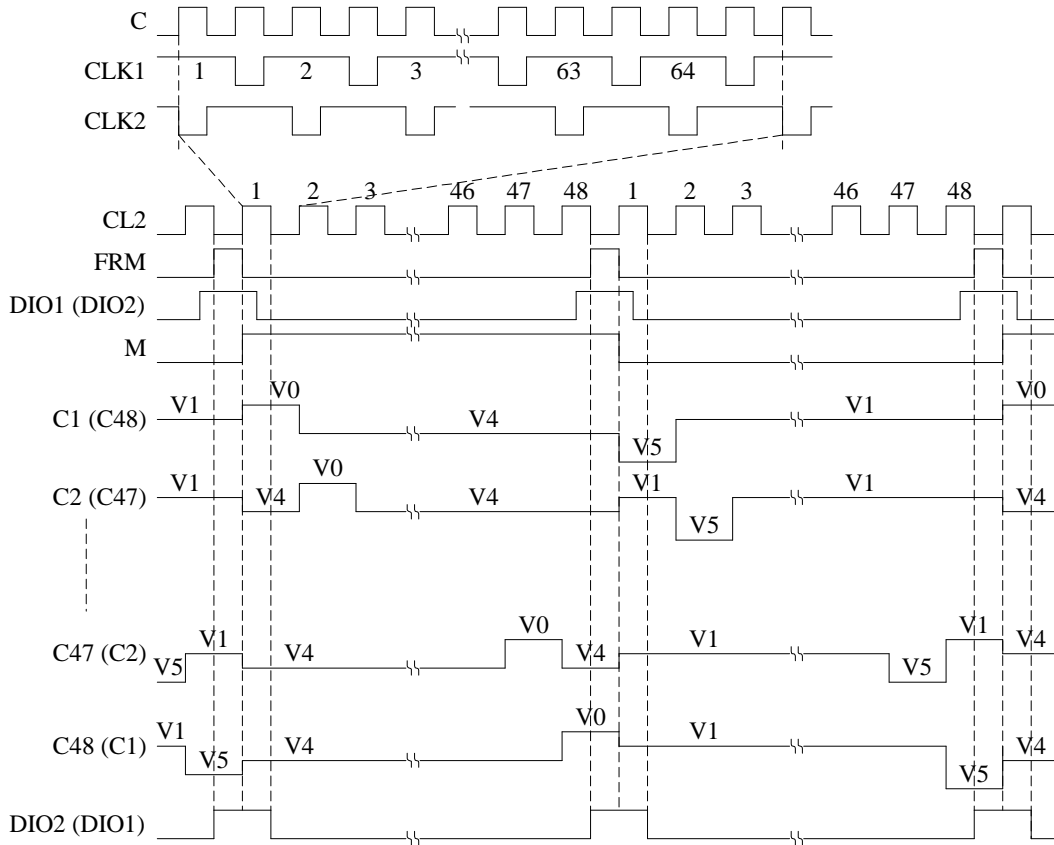
When MS is connected to V<sub>SS</sub>, it depends on the SHL.

<b>MS</b>	<b>SHL</b>	<b>DIO1</b>	<b>DIO2</b>	<b>Direction of Data</b>
H	H	Output	Output	C1 à C64
	L	Output	Output	C64 à C1
L	H	Input	Output	DIO1 à C1 à C64 à DIO2
	L	Output	Input	DIO2 à C64 à C1 à DIO1

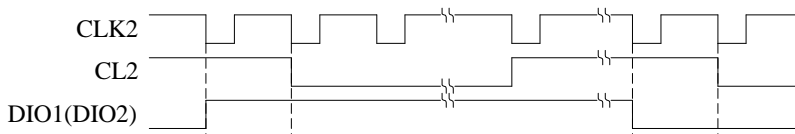
**TIMING DIAGRAM**

**1/48 DUTY TIMING (MASTER MODE)**

Condition: DS1=L, DS2=L, SHL=H (L), PCLK2=H

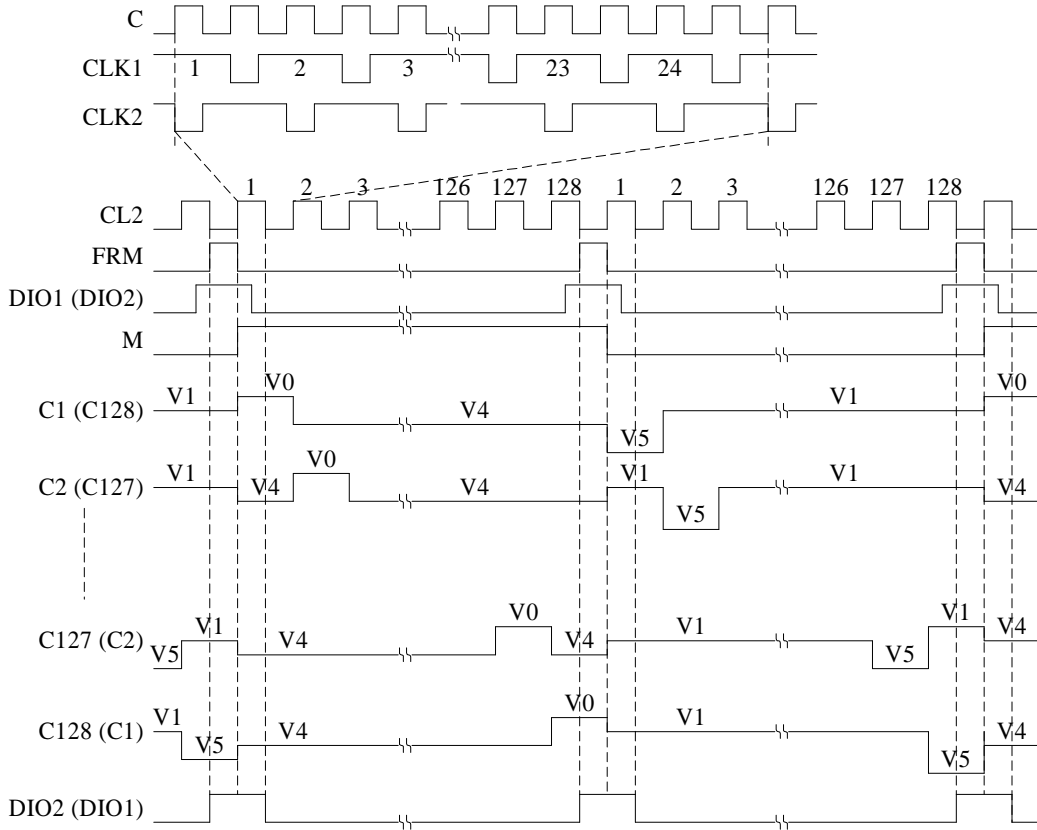


Relation of CL2 and DIO1(DIO2)

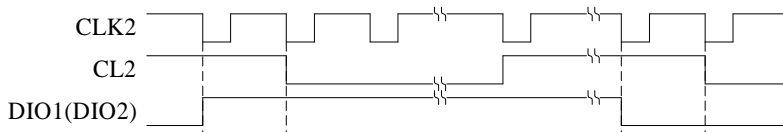


**1/128 DUTY TIMING (MASTER MODE)**

Condition: DS1=H, DS2=H, SHL=H(L), PCLK2=H

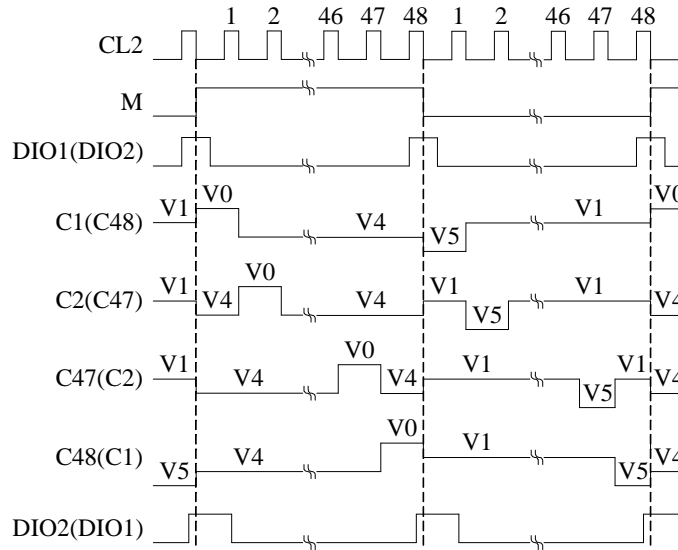


Relation of CL2 and DIO1(DIO2)

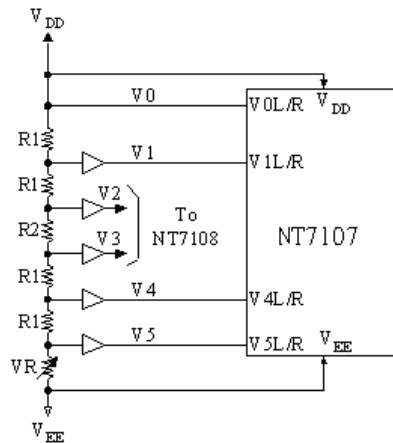


**1/48 DUTY TIMING (SLAVE MODE)**

Condition: SHL=H (L), PCLK2=L



**POWER DRIVER CIRCUIT**



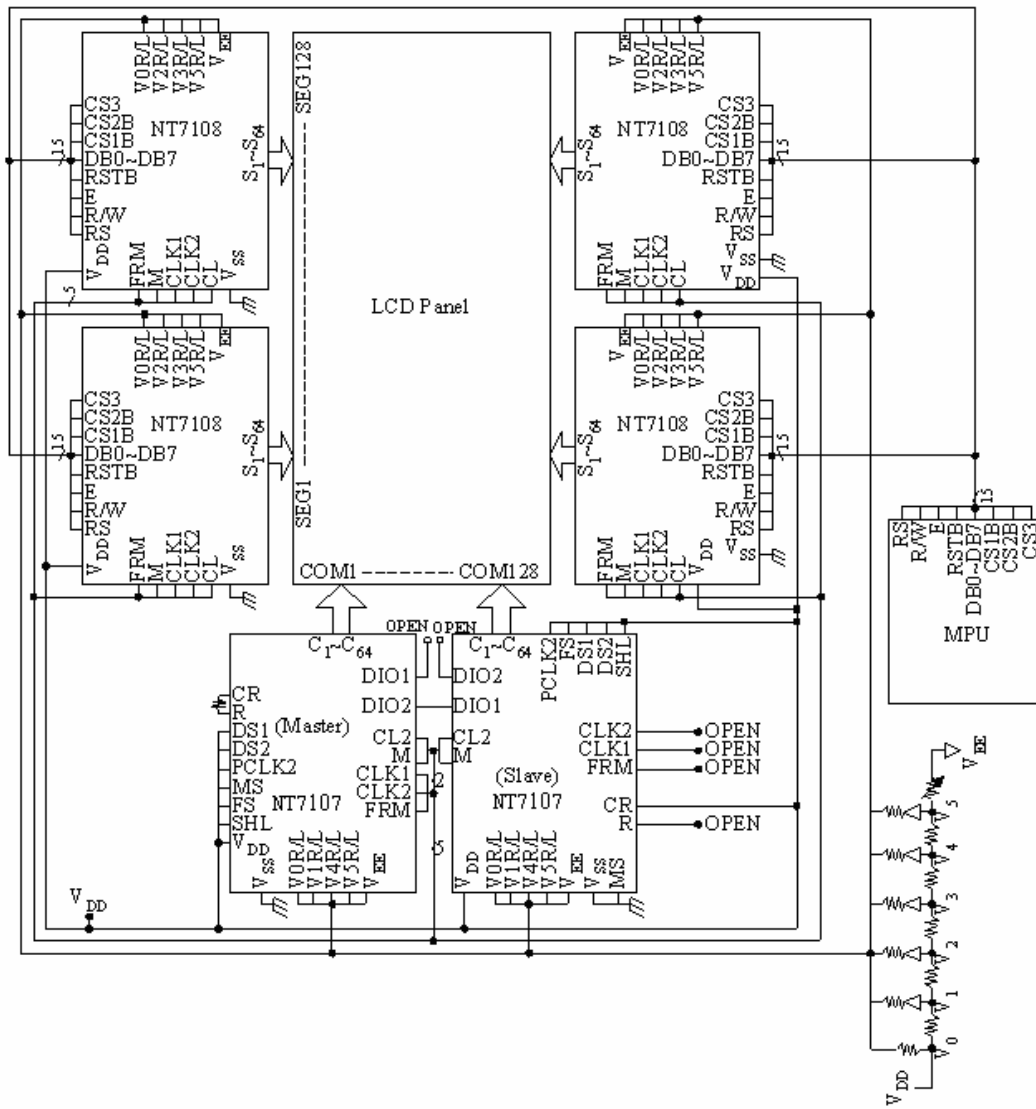
**Relation of Duty & Bias**

Duty	Bias	RDIV
1/48	1/8	R2=4R1
1/64	1/9	R2=5R1
1/96	1/11	R2=7R1
1/128	1/12	R2=8R1

When duty factor is 1/48, the value of R1 & R2 should satisfy.  
 $R1/(4R1 + R2)=1/8$  ;  
 $R1=3k\Omega$  ,  $R2=12k\Omega$

**APPLICATION CIRCUIT**

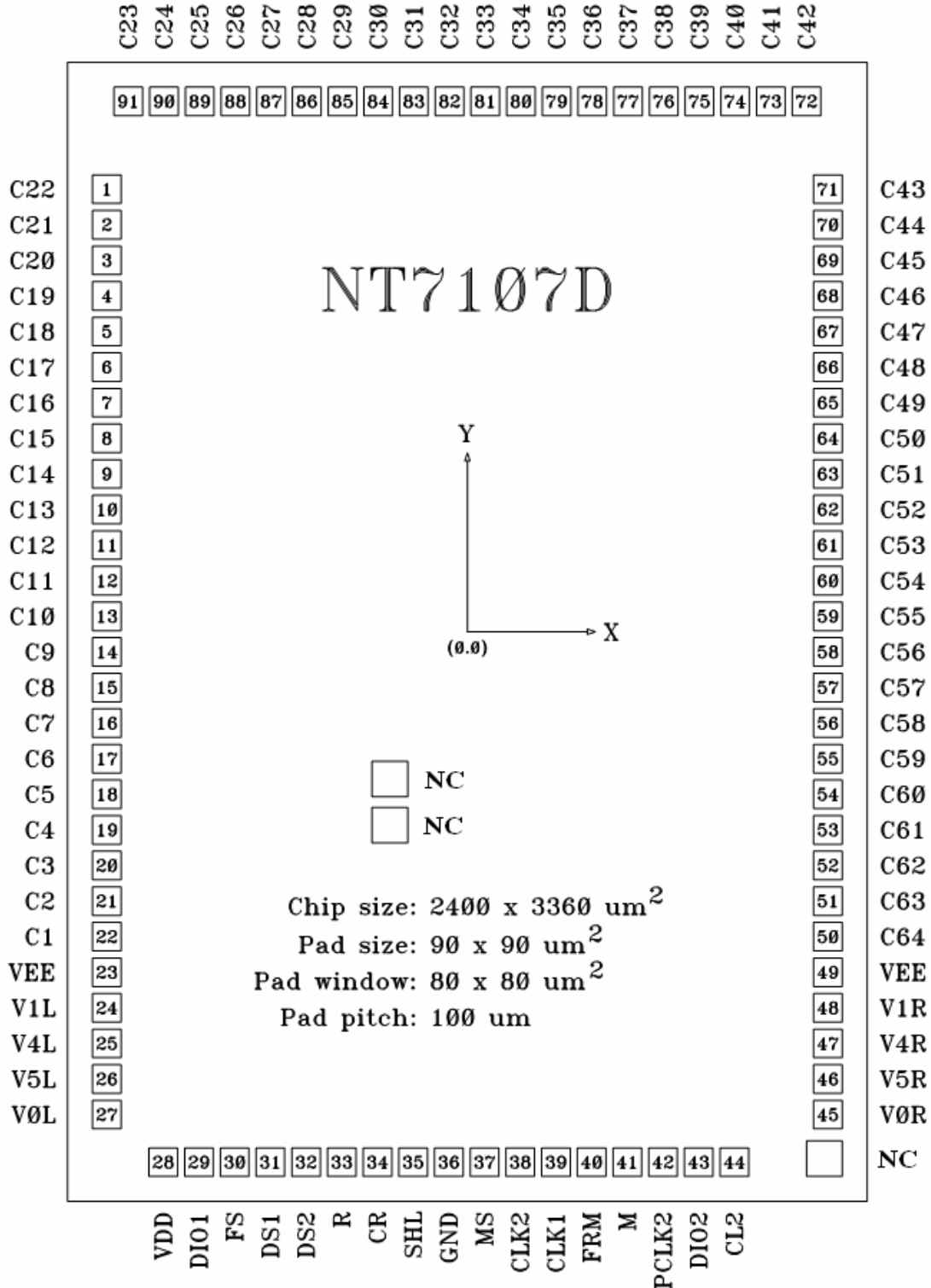
1/128 duty Segment driver (NT7108) interface circuit





PAD DIAGRAM

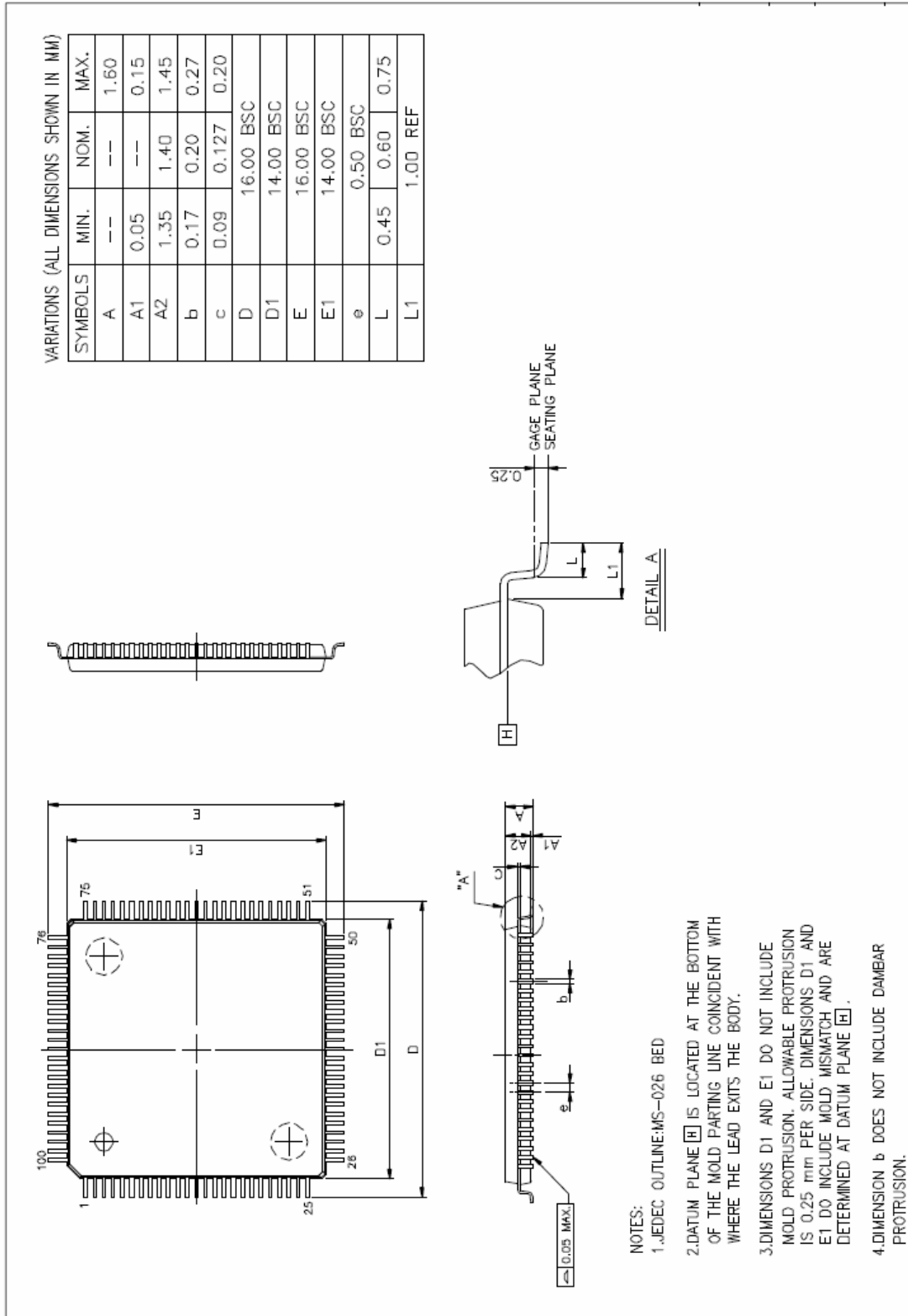
**Note:** Connect the substrate to  $V_{DD}$  or floating.



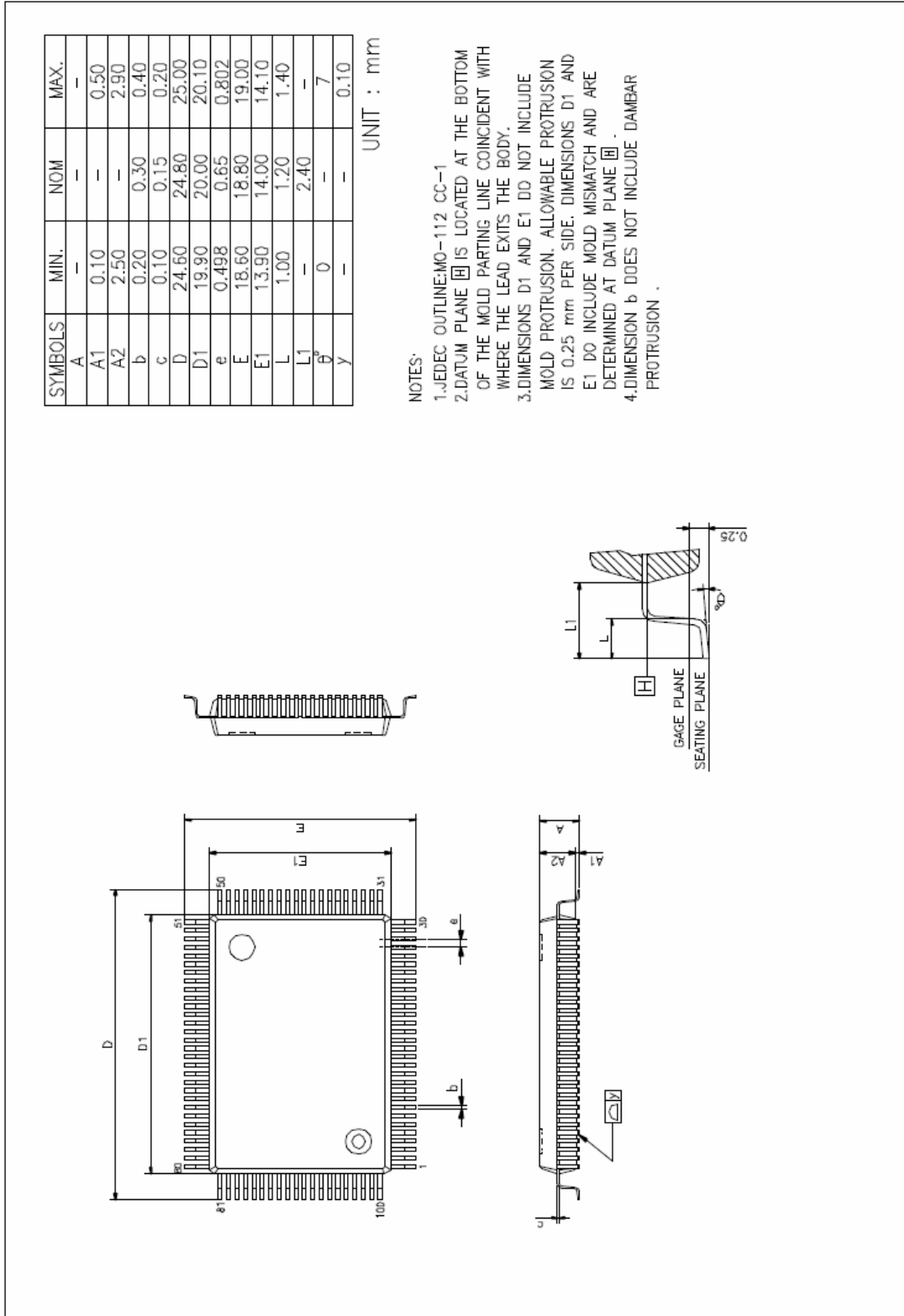
**PAD DIAGRAM**

PAD		COORDINATES		PAD		COORDINATES		PAD		COORDINATES	
N0.	NAME	X	Y	N0.	NAME	X	Y	N0.	NAME	X	Y
1	C22	-1010.0	1243.4	38	CLK2	148.0	-1490.0	75	C39	650.0	1490.0
2	C21	-1010.0	1143.4	39	CLK1	248.0	-1490.0	76	C38	550.0	1490.0
3	C20	-1010.0	1043.4	40	FRM	348.0	-1490.0	77	C37	450.0	1490.0
4	C19	-1010.0	943.4	41	M	448.0	-1490.0	78	C36	350.0	1490.0
5	C18	-1010.0	843.4	42	PCLK2	548.0	-1490.0	79	C35	250.0	1490.0
6	C17	-1010.0	743.4	43	DIO2	648.0	-1490.0	80	C34	150.0	1490.0
7	C16	-1010.0	643.4	44	CL2	748.0	-1490.0	81	C33	50.0	1490.0
8	C15	-1010.0	543.4	45	V0R	1010.0	-1356.6	82	C32	-50.0	1490.0
9	C14	-1010.0	443.4	46	V5R	1010.0	-1256.6	83	C31	-150.0	1490.0
10	C13	-1010.0	343.4	47	V4R	1010.0	-1156.6	84	C30	-250.0	1490.0
11	C12	-1010.0	243.4	48	V1R	1010.0	-1056.6	85	C29	-350.0	1490.0
12	C11	-1010.0	143.4	49	VEE	1010.0	-956.6	86	C28	-450.0	1490.0
13	C10	-1010.0	43.4	50	C64	1010.0	-856.6	87	C27	-550.0	1490.0
14	C9	-1010.0	-56.6	51	C63	1010.0	-756.6	88	C26	-650.0	1490.0
15	C8	-1010.0	-156.6	52	C62	1010.0	-656.6	89	C25	-750.0	1490.0
16	C7	-1010.0	-256.6	53	C61	1010.0	-556.6	90	C24	-850.0	1490.0
17	C6	-1010.0	-356.6	54	C60	1010.0	-456.6	91	C23	-950.0	1490.0
18	C5	-1010.0	-456.6	55	C59	1010.0	-356.6				
19	C4	-1010.0	-556.6	56	C58	1010.0	-256.6				
20	C3	-1010.0	-656.6	57	C57	1010.0	-156.6				
21	C2	-1010.0	-756.6	58	C56	1010.0	-56.6				
22	C1	-1010.0	-856.6	59	C55	1010.0	43.4				
23	VEE	-1010.0	-956.6	60	C54	1010.0	143.4				
24	V1L	-1010.0	-1056.6	61	C53	1010.0	243.4				
25	V4L	-1010.0	-1156.6	62	C52	1010.0	343.4				
26	V5L	-1010.0	-1256.6	63	C51	1010.0	443.4				
27	V0L	-1010.0	-1356.6	64	C50	1010.0	543.4				
28	VDD	-852.0	-1490.0	65	C49	1010.0	643.4				
29	DIO1	-752.0	-1490.0	66	C48	1010.0	743.4				
30	FS	-652.0	-1490.0	67	C47	1010.0	843.4				
31	DS1	-552.0	-1490.0	68	C46	1010.0	943.4				
32	DS2	-452.0	-1490.0	69	C45	1010.0	1043.4				
33	R	-352.0	-1490.0	70	C44	1010.0	1143.4				
34	CR	-252.0	-1490.0	71	C43	1010.0	1243.4				
35	SHL	-152.0	-1490.0	72	C42	950.0	1490.0				
36	VSS	-52.0	-1490.0	73	C41	850.0	1490.0				
37	MS	48.0	-1490.0	74	C40	750.0	1490.0				

**LQFP 100L Outline Dimension**



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*Revision History*

<b>Ver. No</b>	<b>Date</b>	<b>Page</b>	<b>Description</b>
1.0	2015/08/12		First release.