NT7066B

16 COM / 40 SEG DRIVER & CONTROLLER FOR DOT MATRIX LCD

INTRODUCTION

The NT7066B is a dot matrix LCD driver & controller LSI that is fabricated by low CMOS technology.

FUNCTION

- Character type dot matrix LCD driver & controller
- Internal driver : 16 common and 40 segment signal output
- Display character format; 5 x 7 dots + cursor, 5 x 10 dots + cursor
- Easy interface with a 4 bit or 8 bit MPU
- Display character pattern: refer to table 2.
- 5 x 7 dots format 208 kinds, 5 x 10 dots format: 32 kinds
- The special character pattern can be programmable by Character Generator RAM directly
- A customer character pattern can be programmable by mask option.
- Automatic power on reset function.
- It can drive a maximum 80 character by using the NT7065 or NT7063 type.
- It is possible to read both Character Generator and Display Data RAM from MPU.

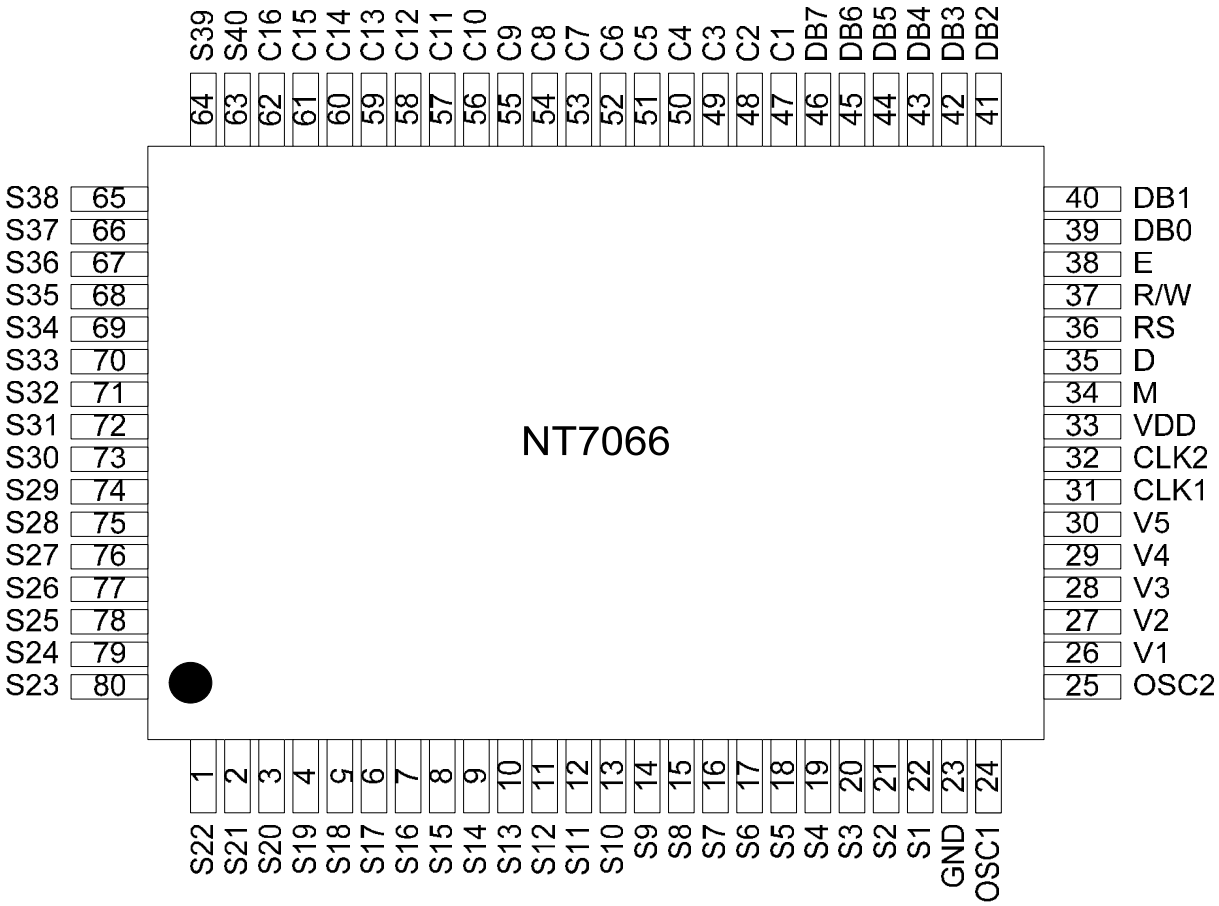
FEATURES

- Internal Memory
  - -Character Generator ROM: 13200 bits
  - -Character Generator RAM: 320 bits
  - -Display Data RAM: 80 x 8bits for 80 digits
- Power Supply Voltage: 2.7V~5.5V
- LCD supply voltage 3~10V (V_{DD} -V_5)
- CMOS process
- 1/8 duty, 1/11 duty or 1/16 duty: selectable
  - -(1/8 duty, 5 x 7 dots format 1 line; 1/11 duty, 5 x 10 dots format 1 line; 1/16 duty, 5x7 format 2 line)
- Bare chip, QFP 80L, LQFP 80L available.

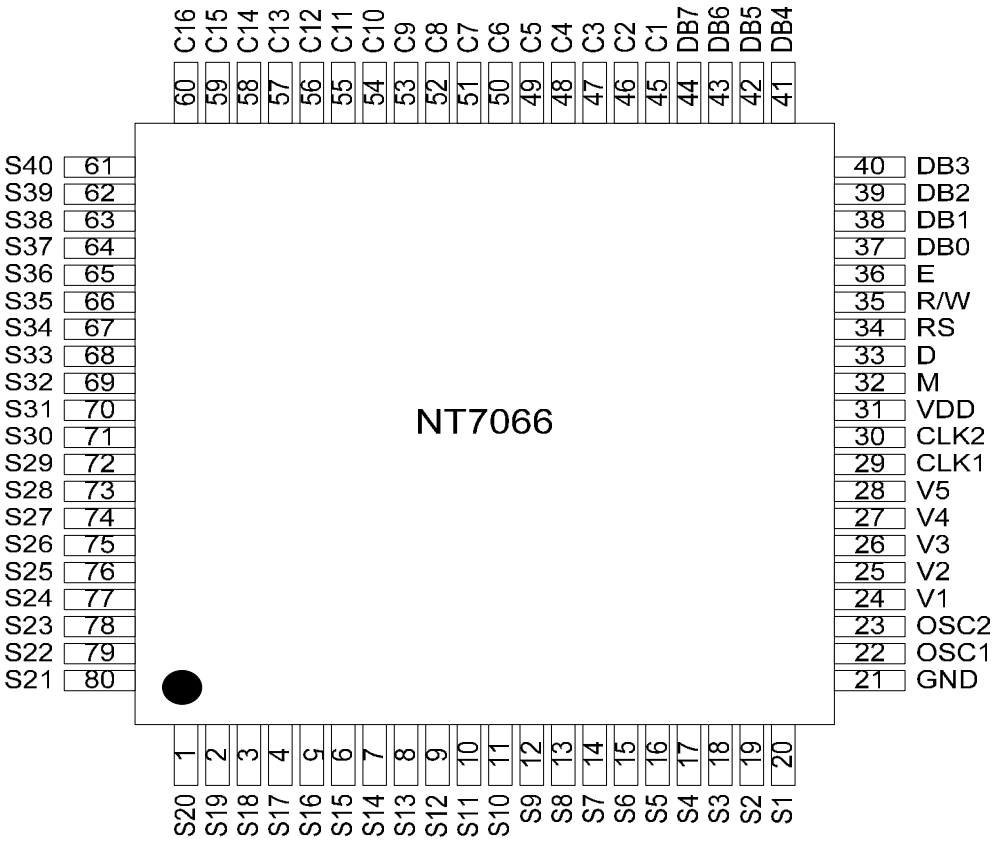
ORDERING INFORMATION

Part No.	Remarks
XXXXXX-F**00**XXXX	English-Japanese character fonts
XXXXXX-F**01**XXXX	English-European character fonts
NT7066B-FXX	Bare Chip
NT7066-FXX**PQFP**	QFP 80L
NT7066-FXX**MQ**	LQFP 80L

PIN CONFIGURATION
QFP 80L

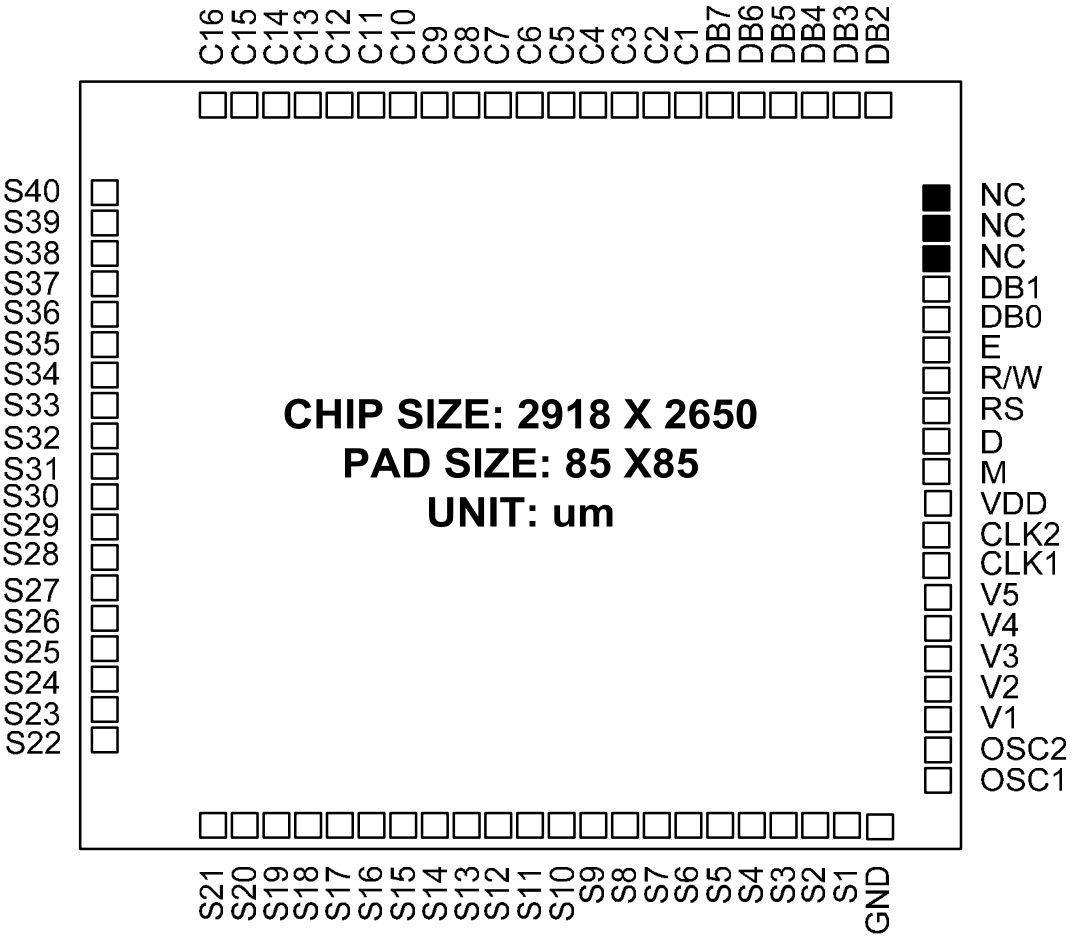


PIN CONFIGURATION
LQFP 80L



PAD DIAGRAM

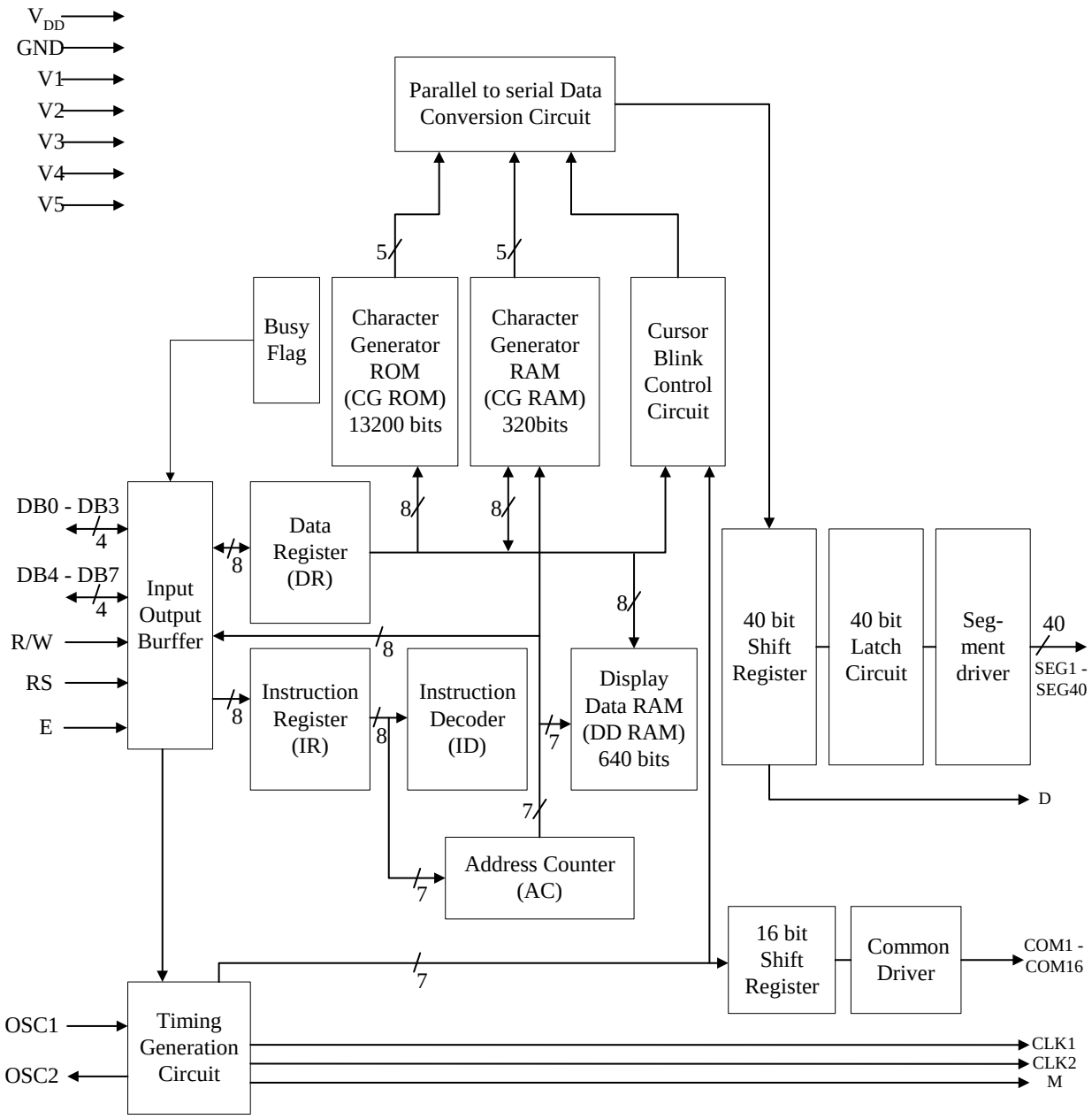
Note: Please connects the substrate to V_{DD} or Floating



PAD LOCATION

Pad number	Signal name	coordinate		Pad number	Signal name	coordinate	
		X(μm)	Y(μm)			X(μm)	Y(μm)
1	S22	81.4	376.35	**41**	DB2	2644.05	2568.6
2	S21	440.29	81.4	**42**	DB3	2539.25	2568.6
3	S20	545.09	81.4	**43**	DB4	2434.05	2568.6
4	S19	650.29	81.4	**44**	DB5	2329.25	2568.6
5	S18	755.09	81.4	**45**	DB6	2224.05	2568.6
6	S17	860.29	81.4	**46**	DB7	2119.25	2568.6
7	S16	965.09	81.4	**47**	C1	2014.05	2568.6
8	S15	1070.29	81.4	**48**	C2	1909.25	2568.6
9	S14	1175.09	81.4	**49**	C3	1804.05	2568.6
10	S13	1280.29	81.4	**50**	C4	1699.25	2568.6
11	S12	1385.09	81.4	**51**	C5	1594.05	2568.6
12	S11	1490.29	81.4	**52**	C6	1489.25	2568.6
13	S10	1595.09	81.4	**53**	C7	1384.05	2568.6
14	S9	1700.29	81.4	**54**	C8	1279.25	2568.6
15	S8	1805.09	81.4	**55**	C9	1174.05	2568.6
16	S7	1910.29	81.4	**56**	C10	1069.25	2568.6
17	S6	2015.09	81.4	**57**	C11	964.05	2568.6
18	S5	2120.29	81.4	**58**	C12	859.25	2568.6
19	S4	2225.09	81.4	**59**	C13	754.05	2568.6
20	S3	2330.29	81.4	**60**	C14	649.25	2568.6
21	S2	2435.09	81.4	**61**	C15	544.05	2568.6
22	S1	2540.29	81.4	**62**	C16	439.25	2568.6
23	GND	2650.19	76	**63**	S40	81.4	2266.35
24	OSC1	2842	236.55	**64**	S39	81.4	2161.55
25	OSC2	2842	341.75	**65**	S38	81.4	2056.35
26	V1	2842	446.75	**66**	S37	81.4	1951.55
27	V2	2842	551.55	**67**	S36	81.4	1846.35
28	V3	2842	656.55	**68**	S35	81.4	1741.55
29	V4	2842	761.55	**69**	S34	81.4	1636.35
30	V5	2842	868.55	**70**	S33	81.4	1531.55
31	CLK1	2836.6	978.55	**71**	S32	81.4	1426.35
32	CLK2	2836.6	1083.75	**72**	S31	81.4	1321.55
33	VDD	2842	1193.3	**73**	S30	81.4	1216.35
34	M	2836.6	1303.25	**74**	S29	81.4	1111.55
35	D	2836.6	1408.05	**75**	S28	81.4	1006.35
36	RS	2836.6	1513.25	**76**	S27	81.4	901.55
37	R/W	2836.6	1618.05	**77**	S26	81.4	796.35
38	E	2836.6	1723.25	**78**	S25	81.4	691.55
39	DB0	2836.6	1828.05	**79**	S24	81.4	586.35
40	DB1	2836.6	1933.25	**80**	S23	81.4	481.55

BLOCK DIAGRAM



PIN DESCRIPTION

PIN(No)	INPUT/ OUTPUT	NAME	DESCRIPTION	INTERFACE
VDD		Operating Voltage	For logic circuit (+3V±10%,+5V±10%)	Power Supply
VSS			0V(GND)	
V1~V5		Driver Supply Voltage	Bias voltage level for LCD driving	
S1~S40	Output	Segment output	Segment signal output for LCD driver	LCD
C1~C16	Output	Common output	Common signal output for LCD driver	LCD
OSC1,OSC2	Input (OSC1), Output (OSC2)	Oscillator	When use internal oscillator, connect the external Rf resister. If external clock is used, connect it to OSC1.	External resister/ Oscillator (OSC1)
CLK1,CLK2	Output	Extension driver latch (CLK1) / shift (CLK2) clock	Each outputs extension driver latch clock and extension driver shift clock	Extension driver
M	Output	Alternated signal for LCD driver output	Outputs the alternating signal to convert LCD driver waveform to AC	Extension driver
D	Output	Display data interface	Outputs extension driver data (the 41th dot's data)	Extension driver
RS	Input	Register select	Used as register selection input. When RS = "High", Data register is selected. When RS = "Low", Instruction register is selected.	MPU
R/W	Input	Read/ Write	Used as read/write selection input. When R/W = "High", read operation. When R/W = "Low", write operation.	MPU
E	Input	Read/ Write enable	Read /write enable signal.	MPU
DB0~DB3	Input / Output	Data bus 0~7	When in 8-bit bus mode, used as low order bi-directional data bus. During 4-bit bus mode open these pins.	MPU
DB4~DB7			When in 8-bit bus mode, used as high order bi-directional data bus. In case of 4-bit bus mode, used as both high and low order. DB7 is used for Busy Flag output.	

FUNCTION DESCRIPTION

System Interface

This chip has all two kinds of interface type with MPU: 4-bit and 8-bit bus.
4-bit bus and 8-bit bus is selected by DL bit in the instruction register.

During read or write operation, two 8-bit registers are used. One is data register (DR), the other is instruction register (IR).

The data register (DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically. So to speak, after MPU reads DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically.

The Instruction register (IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data.

To select register, use RS input pin in 4-bit/8-bit bus mode.

Table 1. Various kinds of operations according to RS and R/W bits.

RS	R/W	Operation
L	L	Instruction Write operation (MPU writes Instruction code into IR)
L	H	Read Busy Flag (DB7) and address counter (DB0~DB6)
H	L	Data Write operation (MPU writes data into DR)
H	H	Data Read operation (MPU reads data from DR)

Busy Flag (BF)

When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and before executing the next instruction, be sure that BF is not High.

Address Counter (AC)

Address Counter (AC) stores DDRAM/CGRAM addresses transferred from IR.
After writing into (reading from)DDRAM/CGRAM, AC is automatically increased (decreased) by 1.
When RS = "Low" and R/W = "High", AC can be read through DB0~DB6 ports.

Display Data RAM (DDRAM)

DDRAM stores display data of maximum 80 x 8 bits (80 characters).
DDRAM address is set in the address counter (AC) as a hexadecimal number. (Refer to Fig.1.)

MSB						LSB
AC6	AC5	AC4	AC3	AC2	AC1	AC0

Fig.1. DDRAM Address

1) 1 line display

In case of 1 line display, the address range of DDRAM is 00H ~ 4FH. Extension driver will be used. Fig.2 shows the example that 40 segment extension driver is added.

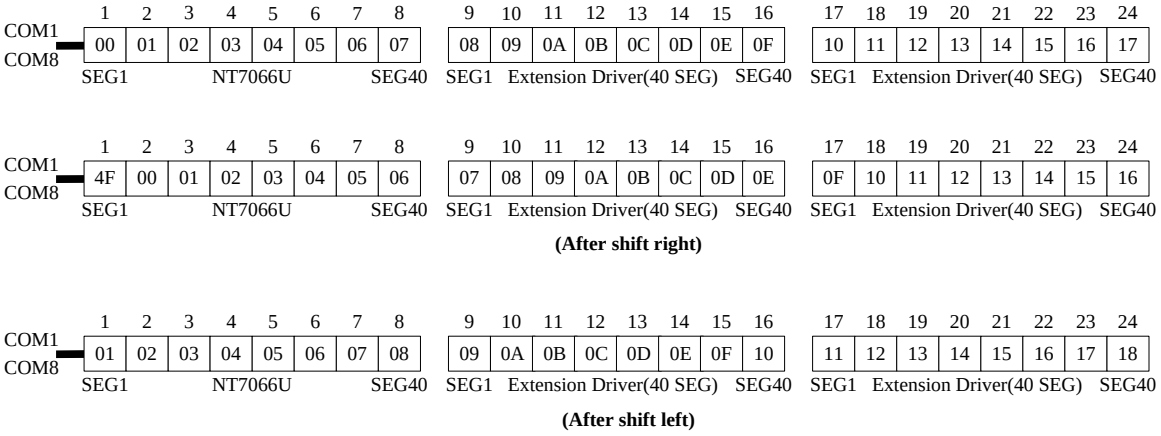


Fig.2. 1-line X 24ch, display with 40 SEG & extension driver.

2) 2 line display

In case of 2 line display, the address range of DDRAM is 00H ~ 27H, 40H ~ 67H. Extension driver will be used. Fig.3 shows the example that 40 segment extension driver is added.

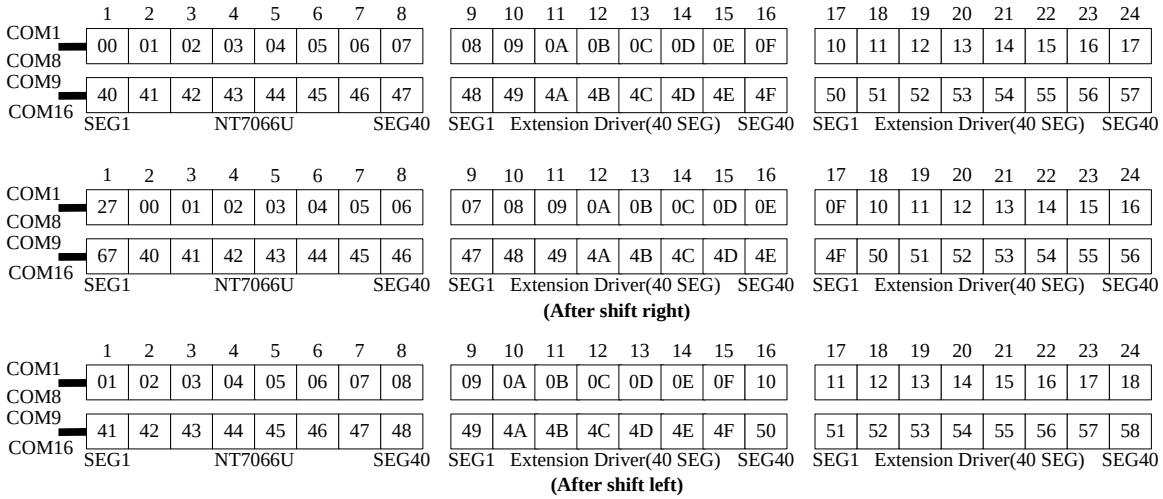


Fig.3. 2-line X 24ch, display with 40 SEG & extension driver.

CGROM (Character Generator ROM)
CGROM has 5 x 8 dot, 208 character, 5 x 11 dot, 32 characters pattern. (Refer to Table 2)

CGRAM (Character Generator RAM)
CGRAM has up to 5 x 8 dot, 8 characters. By writing font data to CGRAM, user defined character can be used. (Refer to Table 3)

Timing Generation Circuit
Timing generation circuit generates clock signals for the internal operations.

LCD Driver Circuit
LCD Driver circuit has 16 common and 40 segment signals for LCD driving.
Data from CGRAM/CGROM is transferred to 40 bits segment latch serially, and then it is stored to 40 bits shift latch. When each common is selected by 16 bits common register, segment data also output through segment driver from 40 bits segment latch.
In case of 1-line display mode, COM1 ~ COM8 have 1/8 duty or COM1 ~ COM11 have 1/11 duty, and in 2-line mode, COM1 ~ COM16 have 1/16 duty ratio.

Cursor/Blink Control Circuit
It controls cursor/blink ON/OFF at cursor position.

Table 2. Standard Character pattern (NT7066-F00)

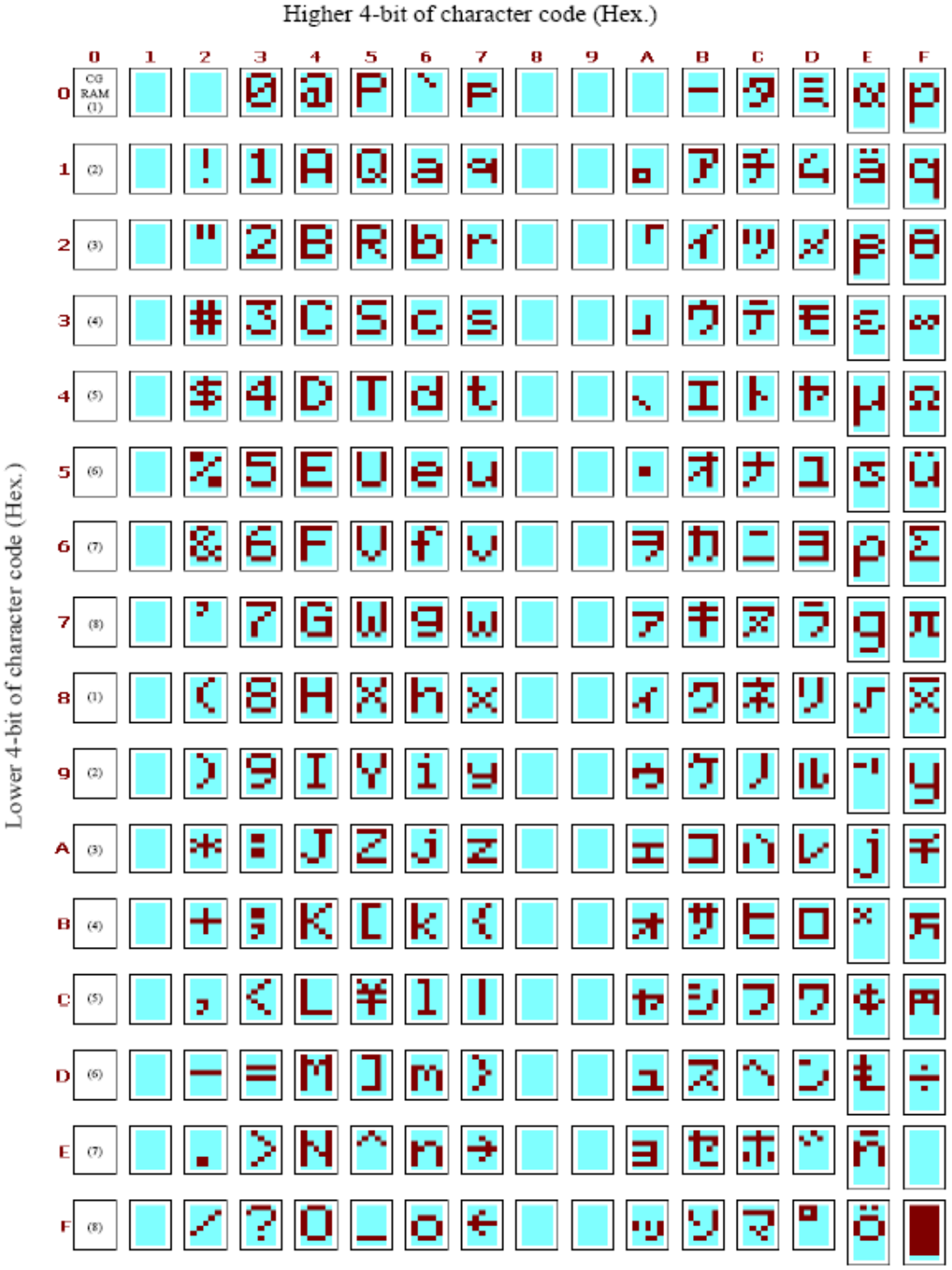


Table 2.1 Standard Character pattern (NT7066-F01)

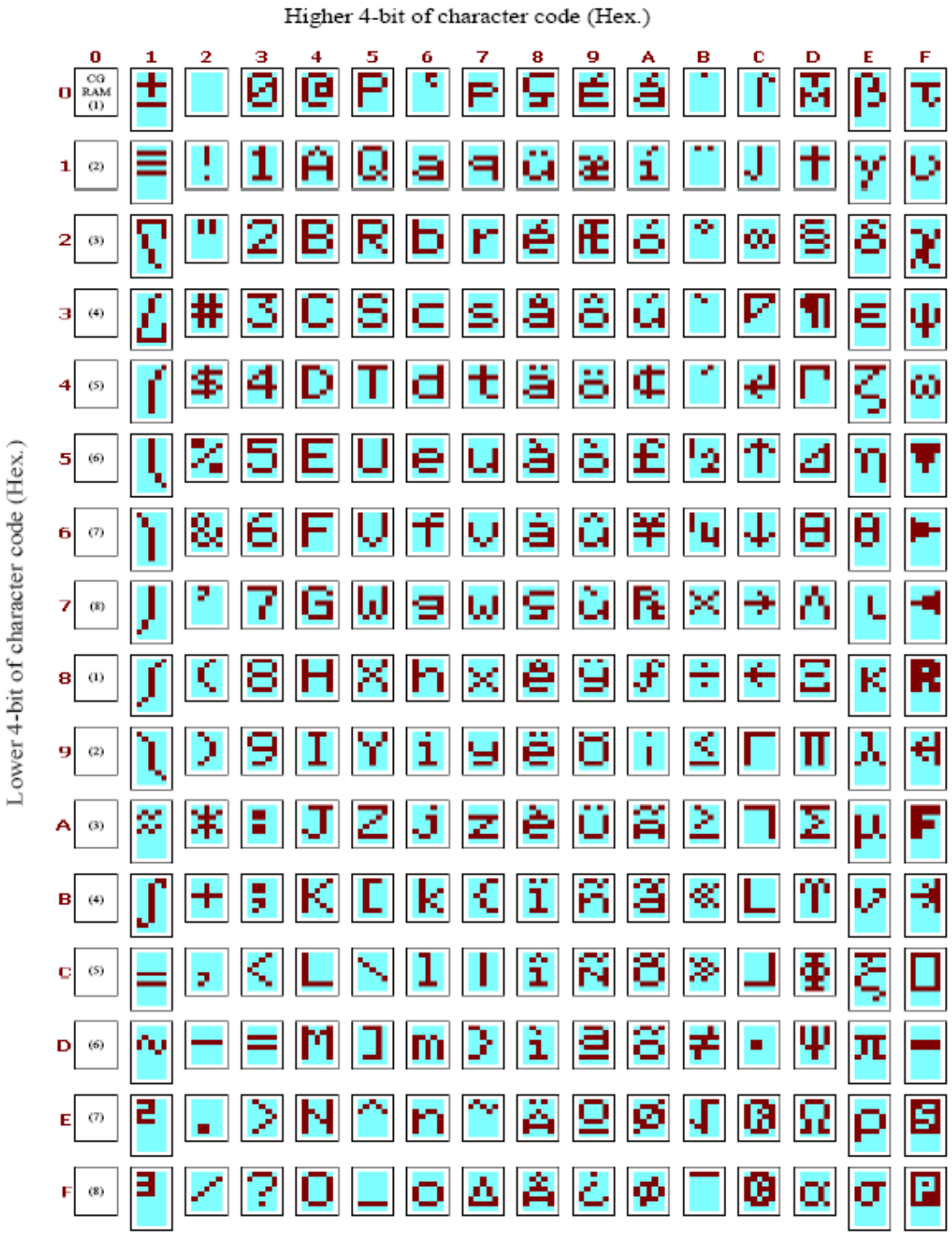


Table 3. Relationship between Character Code(DDRAM) and Character pattern(CGRAM)

Character Code (DDRAM data)								CGRAM address						CGRAM data								Pattern number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	X	0	0	0	0	0	0	0	0	0	X	X	X	0	1	1	1	0	Pattern 1
				.					.		0	0	1		.		1	0	0	0	1	
				.					.		0	1	0		.		1	0	0	0	1	
				.					.		0	1	1		.		1	1	1	1	1	
				.					.		1	0	0		.		1	0	0	0	1	
				.					.		1	0	1		.		1	0	0	0	1	
				.					.		1	1	0		.		1	0	0	0	1	
				.					.		1	1	1		.		0	0	0	0	0	
				.					.			.						.				.
				.					.			.						.				.
				.					.			.						.				.
0	0	0	0	X	1	1	1	1	1	1	0	0	0	X	X	X	1	0	0	0	1	Pattern 8
				.					.		0	0	1		.		1	0	0	0	1	
				.					.		0	1	0		.		1	0	0	0	1	
				.					.		0	1	1		.		1	1	1	1	1	
				.					.		1	0	0		.		1	0	0	0	1	
				.					.		1	0	1		.		1	0	0	0	1	
				.					.		1	1	0		.		1	0	0	0	1	
				.					.		1	1	1		.		0	0	0	0	0	

"X": don't care

INTRODUCTION DESCRIPTION

OUTLINE

To overcome the speed difference between internal clock of NT7066B and MPU clock, NT7066B performs internal operation by storing control information to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and date bus. (Refer to Table 5). Instruction can be divided largely four kinds,

(1) NT7066B function set instructions (set display methods, set data length, etc.)
(2) Address set instructions to internal RAM
(3) Data transfer instructions with internal RAM
(4) Others instructions.

The address of internal RAM is automatically increased or decreased by 1.

*Note: During internal operation, Busy Flag (DB7) is read High. Busy Flag check must precede the next instruction.

Contents

1) Clear Display

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status. Namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

2) Return Home

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	-

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM do not change.

3) Entry Mode Set

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the moving direction of cursor and display.

I/D: Increment / decrement of DDRAM address (cursor or blink)
When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.
When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.
* CGRAM operates the same as DDRAM, when read from or write to CGRAM.

SH: Shift of entire display
When DDRAM read (CGRAM read / write) operation or SH = "Low", shift of entire display is not performed. If SH = "High" and DDRAM write operation, shift of entire display is performed according to I/D value (I/D ="1" : shift left, I/D = "0" : shift right).

4) Display ON/OFF Control

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display / cursor / blink ON / OFF 1 bit register.

D: Display ON / OFF control bit
When D = "High", entire display is turned on.
When D = "Low", display is turned off, but display data is remained in DDRAM.

C: Cursor ON / OFF control bit
When C = "High", cursor is turned on.
When C = "Low", Cursor is disappeared in current display, but I/D register remains its data.

B: Cursor Blink ON / OFF control bit
When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position.
When B = "Low", blink is off.

5) Cursor or Display Shift

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Without Writing or reading of display data, shift right/left cursor position or display. This instruction is used to correct or search display data. (refer to Table 4) During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line. Note that display shift is performed simultaneously in all the line. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed.

Table 4. Shift patterns according to S/C and R/L bits

S/C	R/L	Operation
0	0	Shift the cursor to the left, AC is decreased by 1.
0	1	Shift the cursor to the right, AC is increased by 1.
1	0	Shift all the display to the left, cursor moves according to the display.
1	1	Shift all the display to the right, cursor moves according to the display.

6) Function Set

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	-	-

DL: Interface data length control bit
When DL = "High", it means 8-bit bus mode with MPU.
When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit mode.
When 4-bit bus mode, it needs to transfer 4-bit data by two times.

N: Display line number control bit
When N = "Low", it means 1-line display mode.
When N = "High", 2-line display mode is set.

F: Display font type control bit
When F = "Low", it means 5 x 8 dots format display mode
When F = "High", 5 x11 dots format display mode.

7) Set CGRAM Address

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC. This instruction makes CGRAM data available from MPU.

8) Set DDRAM Address

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.
This instruction makes DDRAM data available from MPU. When 1-line display mode (N = 0), DDRAM address is from "00H" to "4FH". In 2-line display mode (N = 1), DDRAM address is the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

9) Read Busy Flag & Address

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether NT7066B is in internal operation or not. If the resultant BF is “High”, it means the internal operation is in progress and you have to wait until BF to be Low, and then the next instruction can be performed. In this instruction you can read also the value of address counter.

10) Write data to RAM

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM.
The selection of RAM from DDRAM, CGRAM, is set by the previous address set instruction: DDRAM address set, CGRAM address set. RAM set instruction can also determine the AC direction to RAM. After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

11) Read data from RAM

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM.
The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data.
In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction : it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.
In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

Table 5. Instruction Table

Instruction	Instruction Code										Description	Execution time (f_{osc}=270KHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write “20H” to DDRAM and set DDRAM address to “00H” from AC.	1.52ms
Return Home	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to “00H” from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.52ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and make shift of entire display enable.	37μs
Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	Set display(D), cursor(C), and blinking of cursor(B) on/off control bit.	37μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	X	X	Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	37μs
Function Set	0	0	0	0	1	DL	N	F	X	X	Set interface data length(DL:4-bit/8-bit), numbers of display line(N: 1-line/2-line), display font type(F: 5X8 dots/ 5X11 dots)	37μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	37μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	37μs
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or can not be known by reading BF. The contents of address counter can also be read.	0μs
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43μs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43μs

“X”: don’t care

INTERFACE WITH MPU

1) Interface with 8-bits MPU

When interfacing data length is 8-bit, transfer is performed at a time through 8 ports, from DB0 to DB7. Example of timing sequence is shown below.

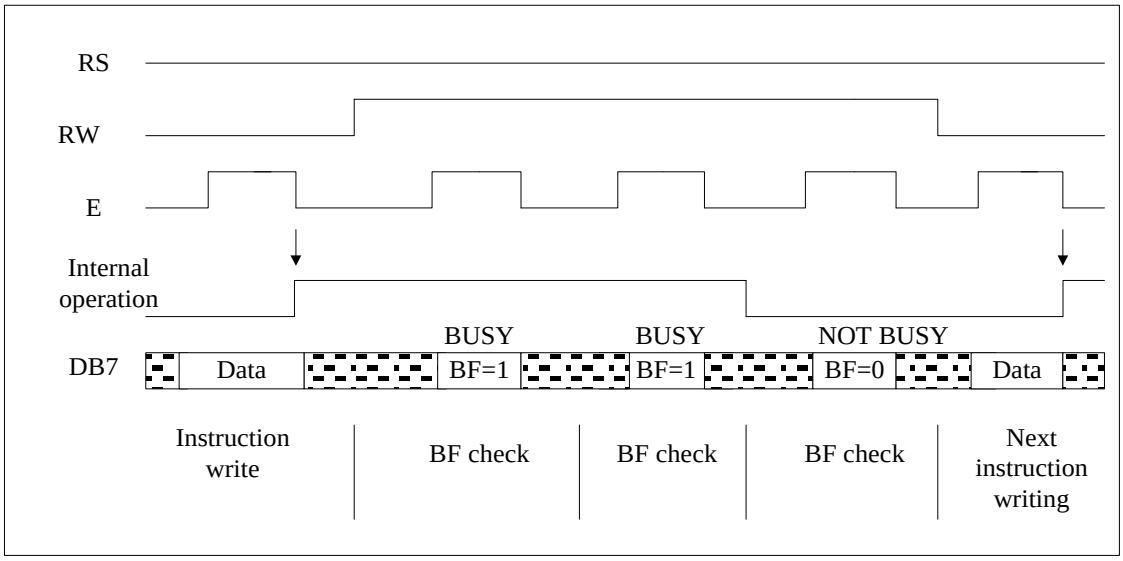


Fig.4. Example of 8-bit Bus Mode Timing Diagram

2) Interface with 4-bits MPU

When interfacing data length is 4-bit, only 4 ports, from DB4 to DB7, are used as data bus. At first higher 4-bit (in case of 8-bit bus mode, the contents of DB4-DB7) are transferred, and then lower 4-bit (in case of 8-bit bus mode, the contents of DB0-BD3) are transferred. So transfer is performed by two times. Busy Flag outputs "High" after the second transfer are ended. Example of timing sequence is shown below.

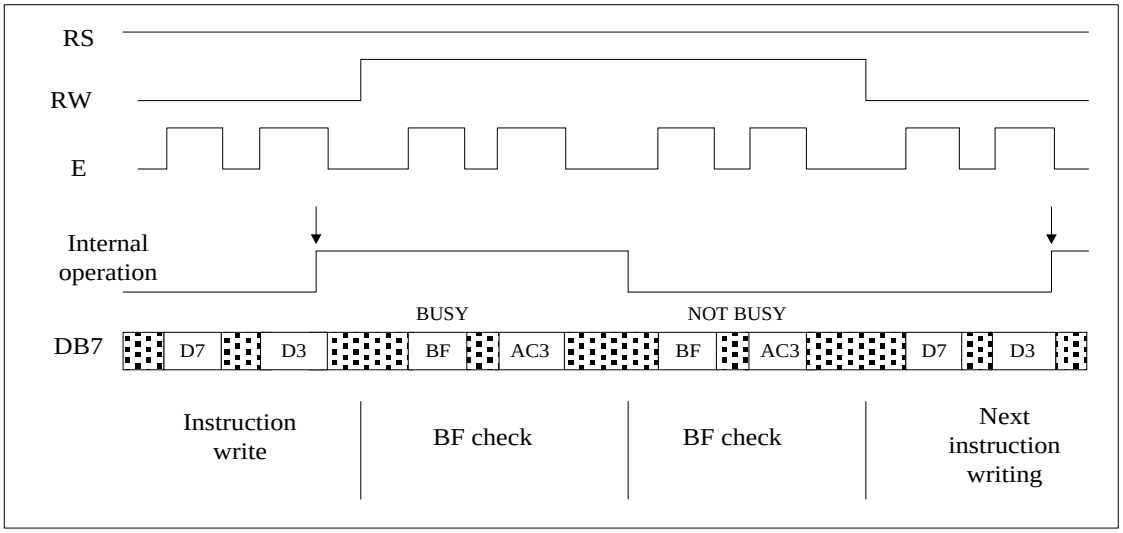
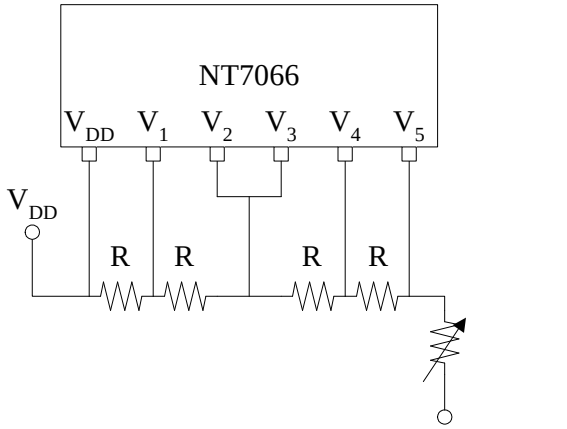
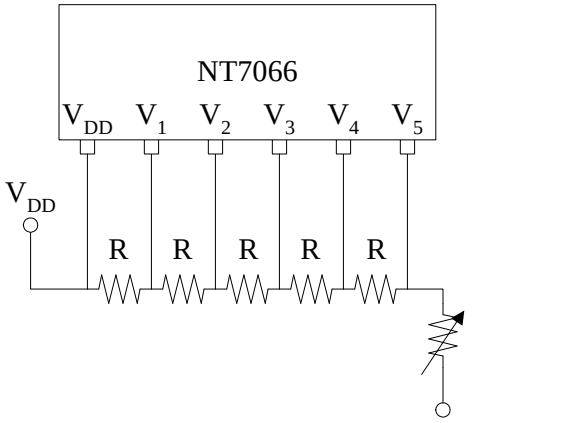


Fig.5. Example of 4-bit Bus Mode Timing Diagram

BIAS VOLTAGE DIVIDE CIRCUIT



(1/4 bias, 1/8 or 1/11 duty)



(1/5 bias, 1/16 duty)

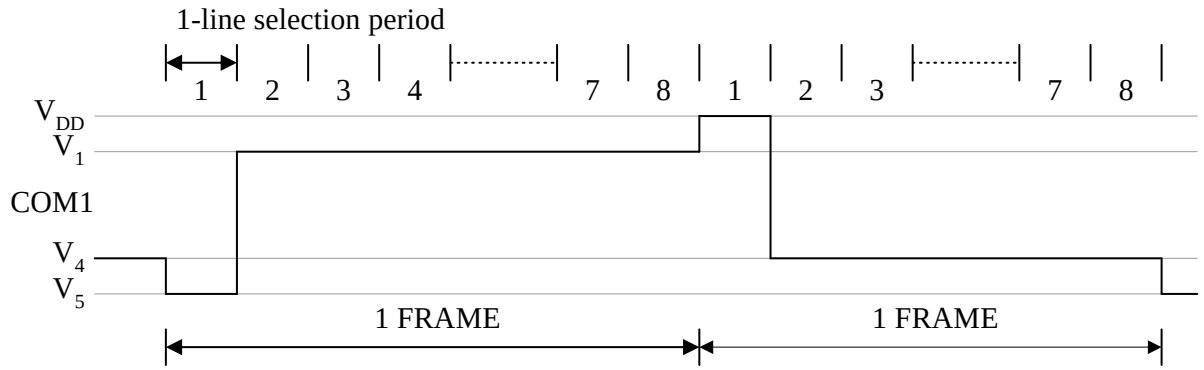
INITIALIZING

When the power is turned on, NT7066B is initialized automatically by power on reset circuit. During the initialization, the following instructions are executed, and BF(Busy Flag)is kept "High"(busy state) to the end of initialization.

1. Display Clear instruction Write "20H" to all DDRAM
2. Set Functions instruction
   - DL=1: 8-bit bus mode
   - N =0: 1-line display mode
   - F =0: 5 x 8 font type
3. Control Display ON/OFF instruction
   - D=0: Display OFF
   - C=0: Cursor OFF
   - B=0: Blink OFF
4. Set Entry Mode instruction
   - I/D=1: Increment by 1
   - SH=0: No entire display shift

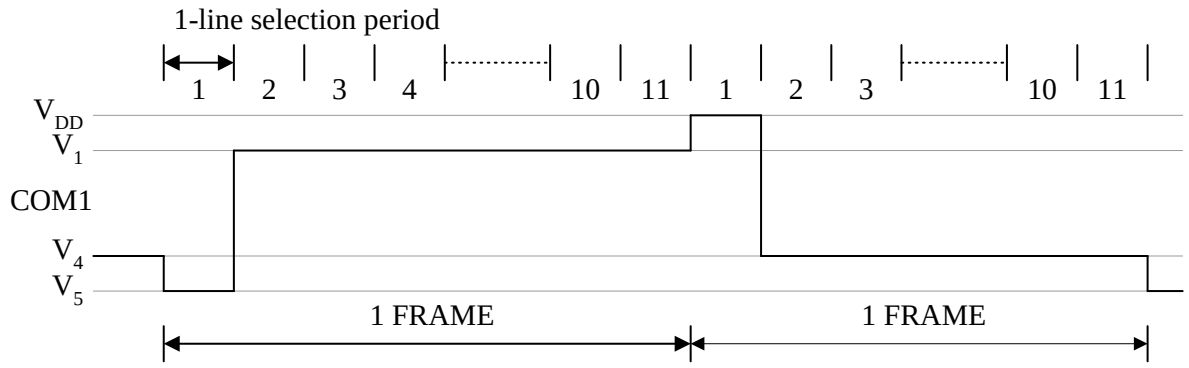
FRAME FREQUENCY

1) 1/8 duty cycle (COM1)



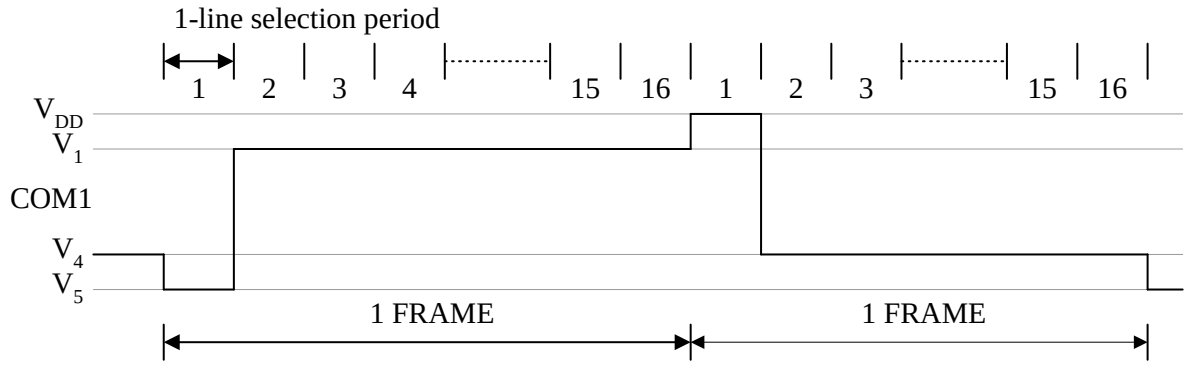
Line selection period = 400 clocks
One Frame = 400 x 8 x 3.7μs =11850 μs =11.9ms (1 clock=3.7μs, fosc=270kHz)
Frame frequency = 1/11.9ms =84.03 Hz

2) 1/11 duty cycle



Line selection period = 400 clocks
One Frame = 400 x 11 x 3.7μs =16300 μs =16.3ms (1 clock=3.7μs, fosc=270kHz)
Frame frequency = 1/16.3ms =61.4 Hz

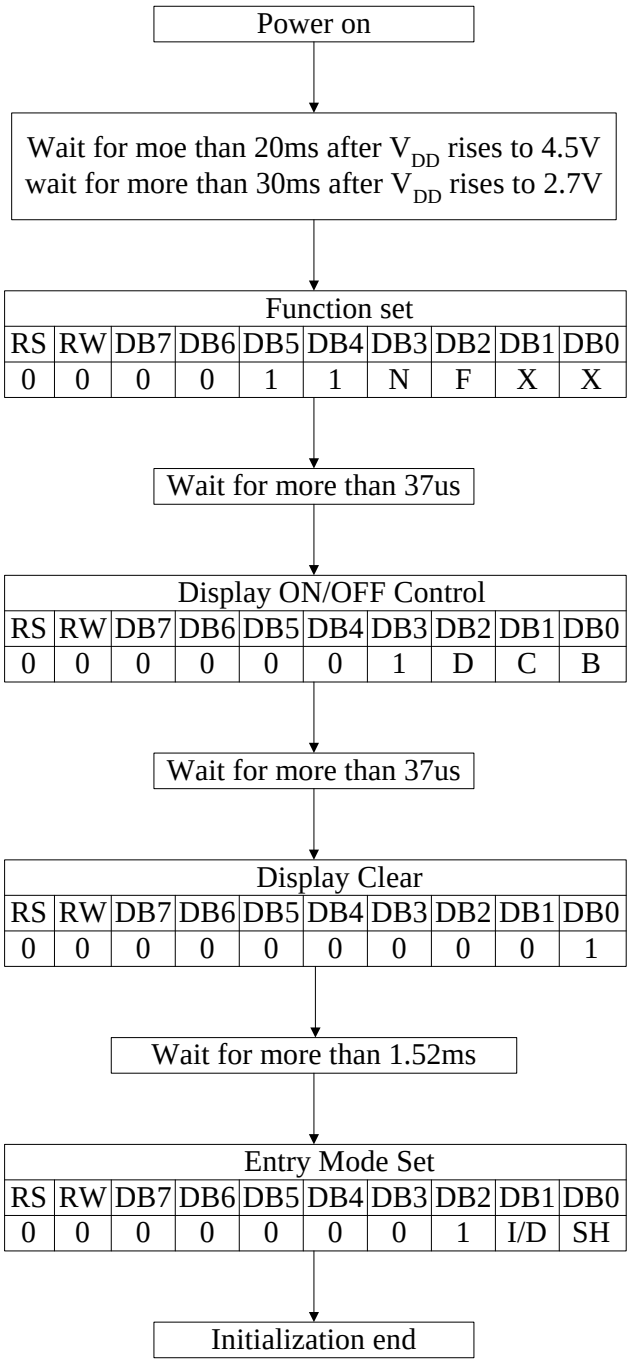
3) 1/16 duty cycle



Line selection period = 200 clocks
One Frame = 200 x 16 x 3.7μs =11850 μs =11.9 ms (1 clock = 3.7μs, fosc=270kHz)
Frame frequency = 1/11.9 ms = 84.03 Hz

INITIALIZING BY INSTRUCTION

1) 8-bit interface mode



Condition: f_{OSC}= 270KHz

N	0	1-line mode
	1	2-;ine mode

F	0	5X8 dots
	1	5X11 dots

D	0	display off
	1	display on

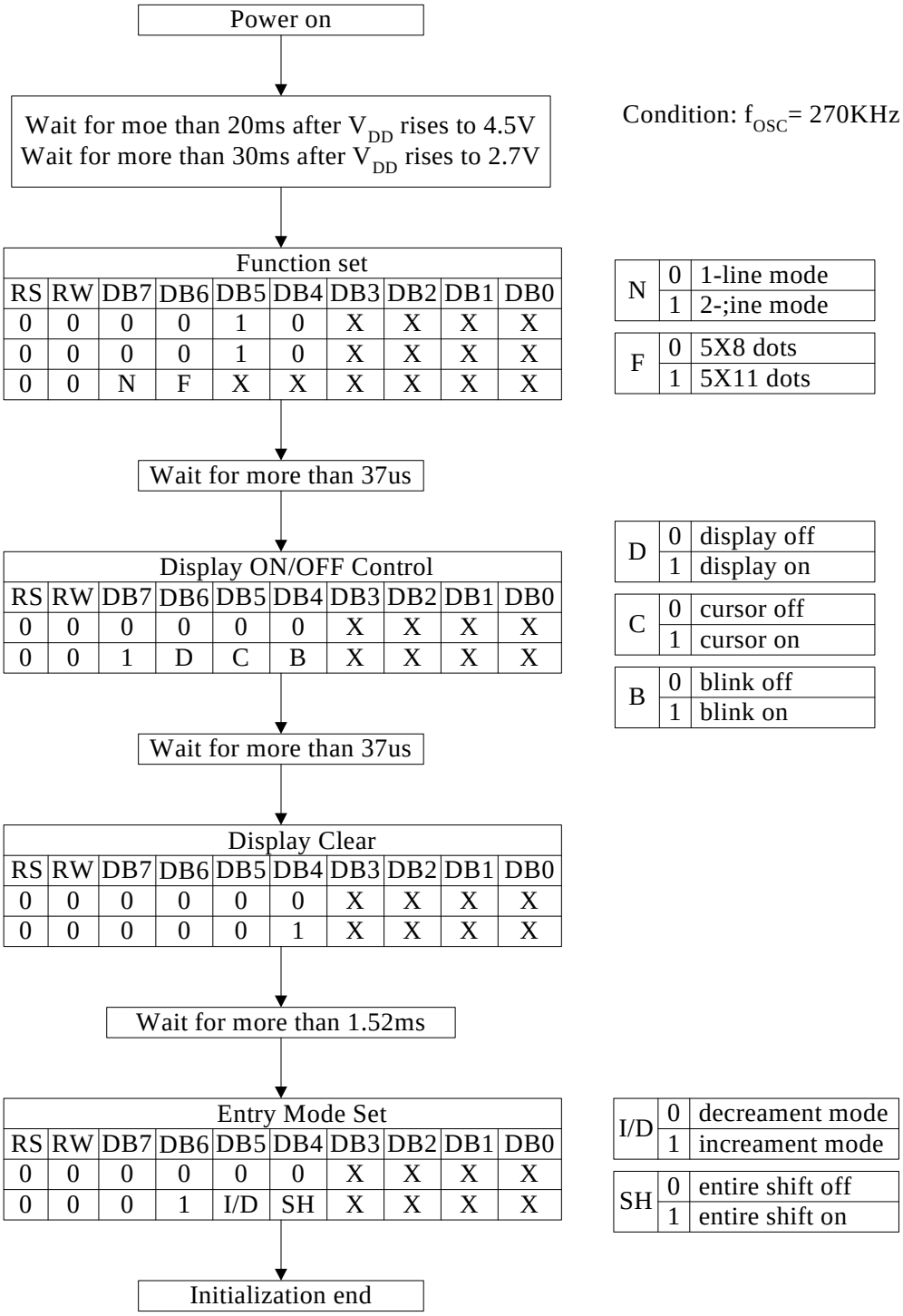
C	0	cursor off
	1	cursor on

B	0	blink off
	1	blink on

I/D	0	decreament mode
	1	increament mode

SH	0	entire shift off
	1	entire shift on

2) 4-bit interface mode



MAXIMUM ABSOLUTE LIMIT

Maximum Absolute Power Ratings

Characteristics	Symbol	Unit	Value
Operating voltage	V_{DD}	V	-0.3 ~ +7.0
Power supply voltage	V_{LCD}	V	V_{DD}-15.0 ~ V_{DD}+0.3
Input voltage	V_{IN}	V	-0.3 ~ V_{DD}+0.3

※ Voltage greater than above may damage the circuit ($V_{DD} \geqq V1 \geqq V2 \geqq V3 \geqq V4 \geqq V5$)

Temperature Characteristics

Characteristics	Symbol	Unit	Value
Operating temperature	T_{OPR}	℃	-30 ~ +85
Storage temperature	T_{STG}	℃	-55 ~ +125

ELECTRICAL CHARACTERISTICS

DC characteristics (V_{DD} = 4.5V~5.5V, Ta = -30~+85℃)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD}	-	4.5	-	5.5	V
Operating current	I_{DD}	Internal oscillation or external clock (V_{DD}=5.0V, f_{OSC}=270KHz)	-	0.35	0.6	mA
Input voltage(1) (except OSC1)	V_{IH1}	-	2.2	-	V_{DD}	V
	V_{IL1}	-	-0.3	-	0.6	
Input voltage(2) (OSC1)	V_{IH2}	-	V_{DD}-1.0	-	V_{DD}	V
	V_{IL2}	-	-0.2	-	1.0	
Output voltage(1) (DB0 to DB7)	V_{OH1}	I_{OH}=-0.205mA	2.4	-	-	V
	V_{OL1}	I_{OL}=1.2mA	-	-	0.4	
Output voltage(2) (except DB0 to DB7)	V_{OH2}	I_O=-40μA	0.9V_{DD}	-	-	V
	V_{OL2}	I_O=40μA	-	-	0.1V_{DD}	
Voltage drop	Vd_{COM}	I_O=±0.1mA	-	-	1	V
	Vd_{SEG}		-	-	1	
Input leakage current	I_{LKG}	V_{IN}=0V ~ V_{DD}	-1	-	1	μA
Input low current	I_{IL}	V_{IN}=0V, V_{DD}=5V (PULL UP)	-50	-125	-150	
Internal clock (external R_f)	f_{OSC1}	Rf=91KΩ±2% (V_{DD}=5V)	190	270	350	KHz
External clock	f_{OSC}	-	125	270	350	
	Duty		45	50	55	%
	t_R, t_F		-	-	0.2	μs
LCD driving voltage	V_{LCD}	V_{DD}-V_5 (1/5, 1/4 bias)	3.0	-	10.0	V

DC characteristics (V_{DD} = 2.7V~4.5V, Ta = -30~+85℃)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD}	-	2.7	-	4.5	V
Operating current	I_{DD}	Internal oscillation or external clock (V_{DD}=3.0V, f_{OSC}=270KHz)	-	0.15	0.3	mA
Input voltage(1) (except OSC1)	V_{IH1}	-	0.7V_{DD}	-	V_{DD}	V
	V_{IL1}	-	-0.3	-	0.55	
Input voltage(2) (OSC1)	V_{IH2}	-	0.7V_{DD}	-	V_{DD}	V
	V_{IL2}	-	-	-	0.2V_{DD}	
Output voltage(1) (DB0 to DB7)	V_{OH1}	I_{OH}=-0.1mA	0.75V_{DD}	-	-	V
	V_{OL1}	I_{OL}=0.1mA	-	-	0.2 V_{DD}	
Output voltage(2) (except DB0 to DB7)	V_{OH2}	I_O=-40μA	0.8V_{DD}	-	-	V
	V_{OL2}	I_O=40μA	-	-	0.2V_{DD}	
Voltage drop	Vd_{COM}	I_O=±0.1mA	-	-	1	V
	Vd_{SEG}		-	-	1	
Input leakage current	I_{LKG}	V_{IN}=0V ~ V_{DD}	-1	-	1	μA
Input low current	I_{IL}	V_{IN}=0V, V_{DD}=3V (PULL UP)	-10	-50	-120	
Internal clock (external R_f)	f_{OSC1}	Rf=75KΩ±2% (V_{DD}=3V)	190	270	350	KHz
External clock	f_{OSC}	-	125	270	350	
	Duty		45	50	55	%
	t_R, t_F		-	-	0.2	μs
LCD driving voltage	V_{LCD}	V_{DD}-V_5 (1/5, 1/4 bias)	3.0	-	10.0	V

AC Characteristics

(V_{DD} = 4.5V~5.5V, Ta = -30~+85℃)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write mode (refer to Fig.6)	E cycle time	t_C	500	-	-	ns
	E rise/fall time	t_R, t_F	-	-	20	
	E pulse width (high, low)	t_W	230	-	-	
	R/W and RS setup time	t_{SU1}	40	-	-	
	R/W and RS hold time	t_{H1}	10	-	-	
	Data setup time	t_{SU2}	60	-	-	
	Data hold time	t_{H2}	10	-	-	
Read mode (refer to Fig.7)	E cycle time	t_C	500	-	-	ns
	E rise/fall time	t_R, t_F	-	-	20	
	E pulse width (high, low)	t_W	230	-	-	
	R/W and RS setup time	t_{SU}	40	-	-	
	R/W and RS hold time	t_H	10	-	-	
	Data output delay time	t_D	-	-	120	
	Data hold time	t_{DH}	5	-	-	

(V_{DD} = 2.7V~4.5V, Ta = -30~+85℃)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write mode (refer to Fig.6)	E cycle time	t_C	1000	-	-	ns
	E rise/fall time	t_R, t_F	-	-	25	
	E pulse width (high, low)	t_W	450	-	-	
	R/W and RS setup time	t_{SU1}	60	-	-	
	R/W and RS hold time	t_{H1}	20	-	-	
	Data setup time	t_{SU2}	195	-	-	
	Data hold time	t_{H2}	10	-	-	
Read mode (refer to Fig.7)	E cycle time	t_C	1000	-	-	ns
	E rise/fall time	t_R, t_F	-	-	25	
	E pulse width (high, low)	t_W	450	-	-	
	R/W and RS setup time	t_{SU}	60	-	-	
	R/W and RS hold time	t_H	20	-	-	
	Data output delay time	t_D	-	-	360	
	Data hold time	t_{DH}	5	-	-	

(V_{DD} = 2.7V~4.5V, Ta = -30~+85℃)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Interface mode with extension driver (refer to Fig.8)	Clock pulse width (high, low)	t_W	800	-	-	ns
	Clock rise/ fall time	t_R, t_F	-	-	25	
	Clock setup time	t_{SU1}	500	-	-	
	Data setup time	t_{SU2}	300	-	-	
	Data hold time	t_{DH}	300	-	-	
	M delay time	t_{DM}	-1000	-	1000	

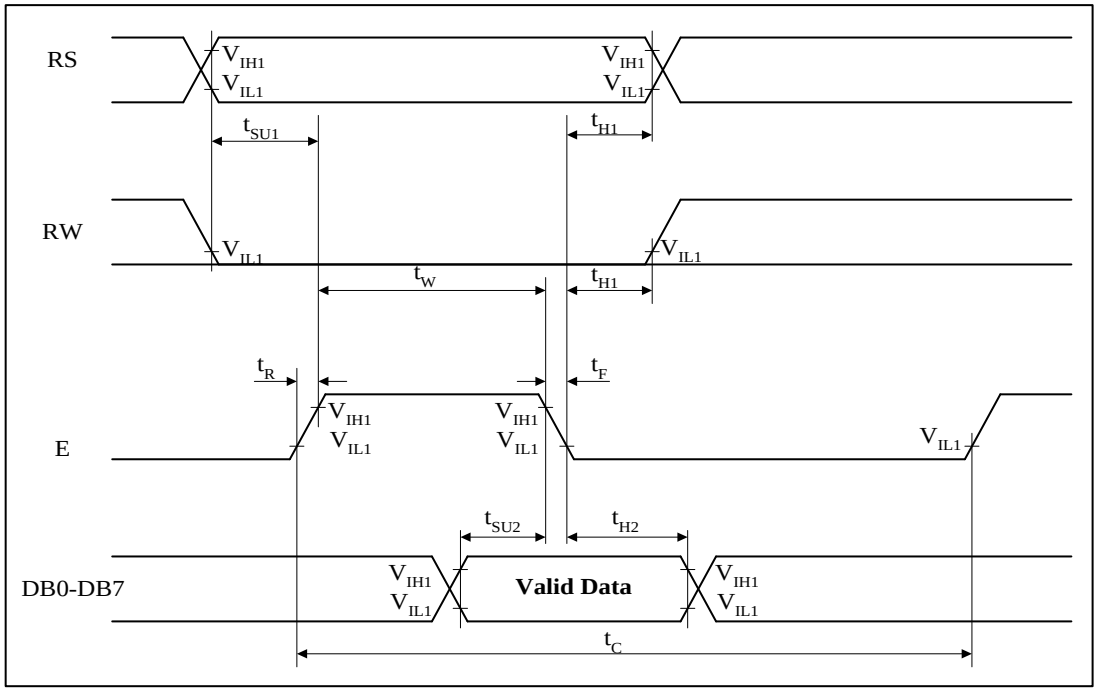


Fig.6. Write mode timing diagram

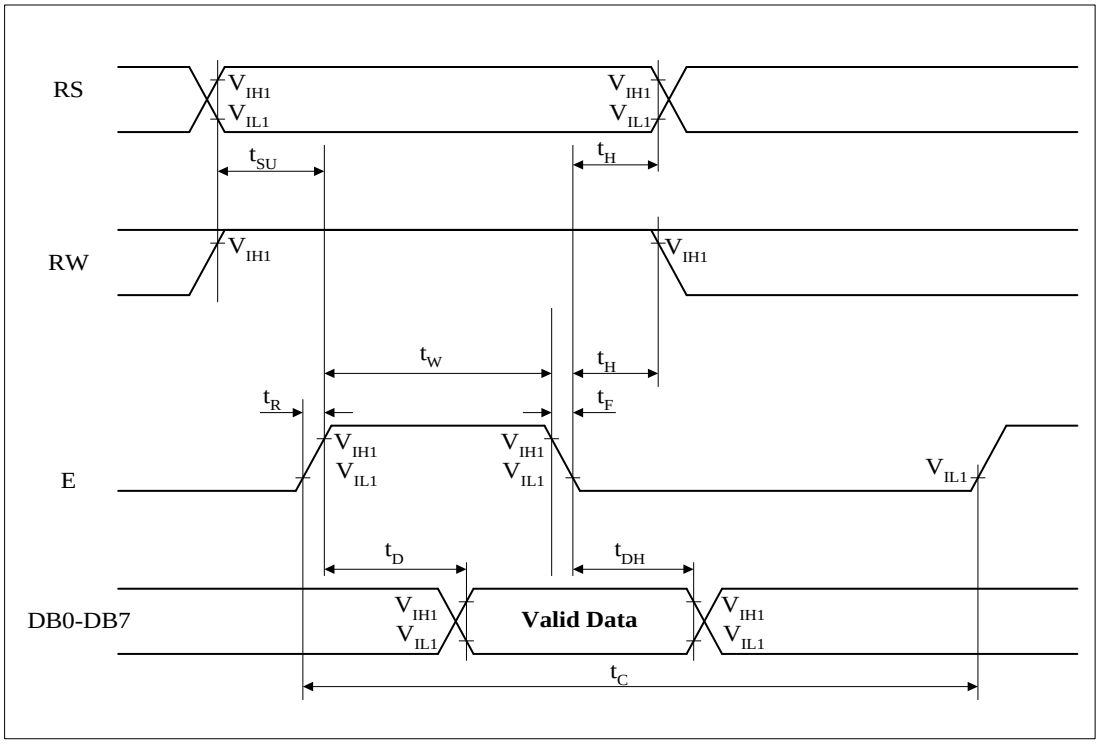


Fig.7. Read mode timing diagram

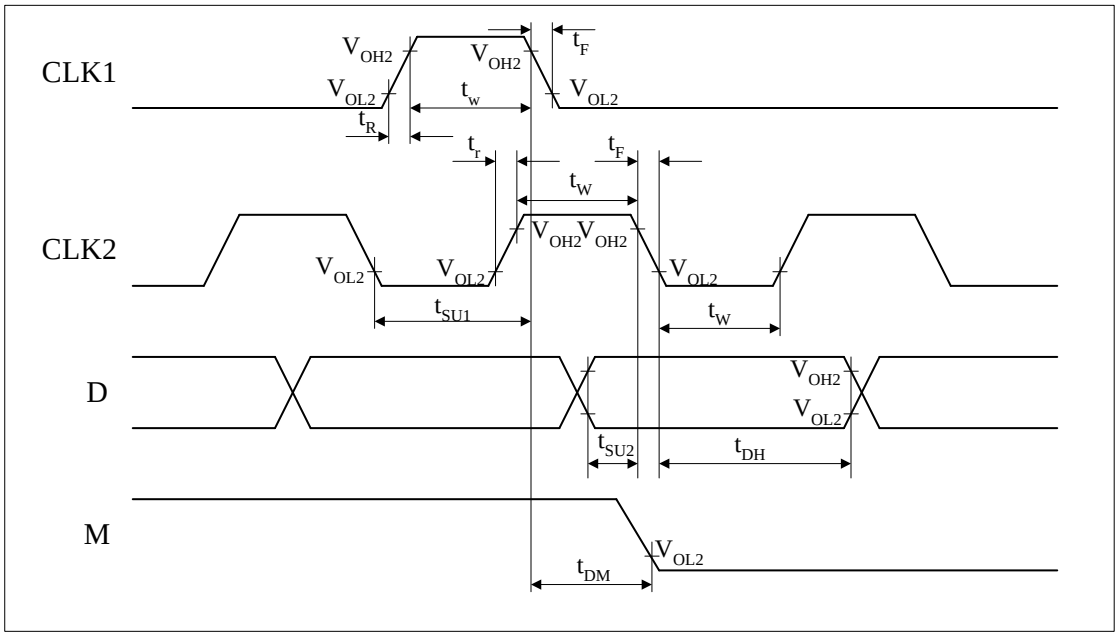
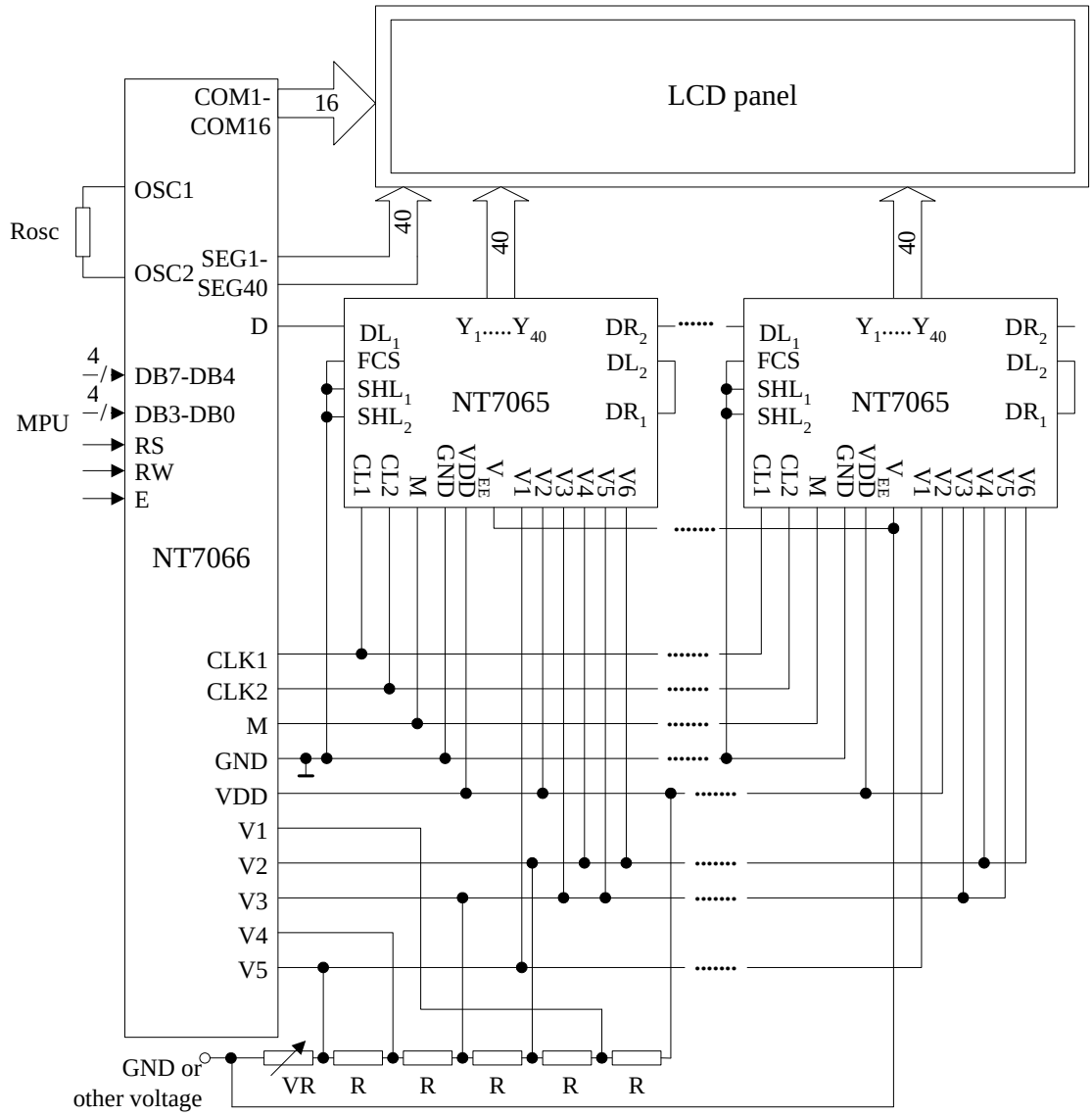


Fig.8. Interface mode with extension driver timing diagram

Application circuit of NT7066B



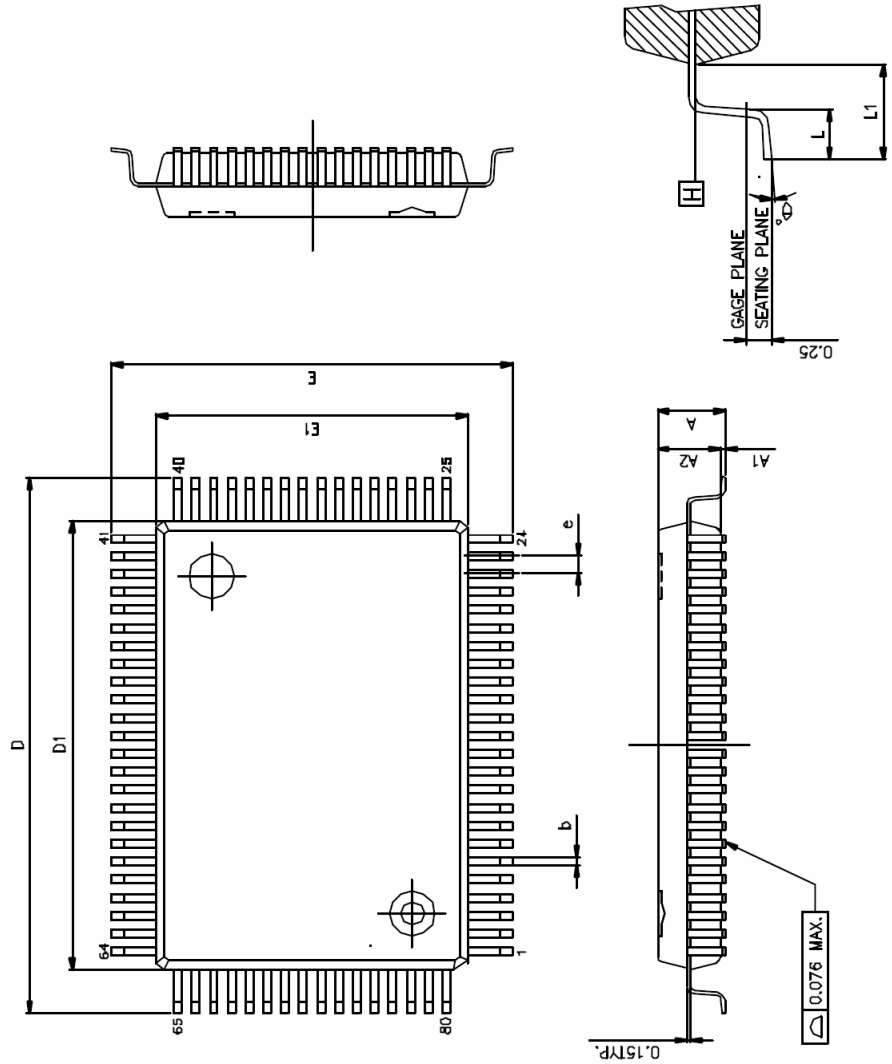
When NT7065 is externally connected to NT7066, you can increase the number of display digits up to 80 characters.

OUTLINE DRAWING (QFP 80L)

SYMBOLS	MIN.	NOM	MAX.
A	–	–	3.40
A1	0.25	–	–
A2	2.55	2.80	3.05
b	0.30	–	0.45
D		23.90 BASIC	
D1		20.00 BASIC	
e		0.8 BASIC	
E		17.90 BASIC	
E1		14.00 BASIC	
L	0.73	0.88	1.03
L1		1.95 REF.	
θ°	0	3.5	7

UNIT : mm

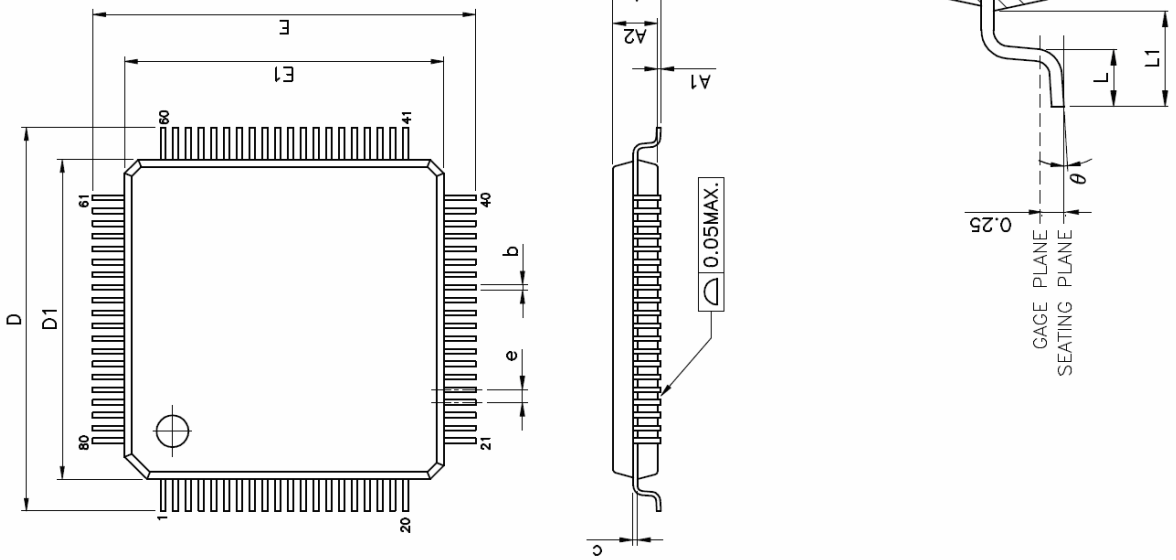
NOTES:
1.JEDEC OUTLINE:MO-112 CB-1
2.DATUM PLANE [H] IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [H]
4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION .



OUTLINE DRAWING (LQFP 80L)

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)			
SYMBOLS	MIN.	NOM.	MAX.
A	---	---	1.60
A1	0.05	---	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	---	0.20
D		12.00 BSC	
D1		10.00 BSC	
E		12.00 BSC	
E1		10.00 BSC	
e		0.40 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

NOTES:
1.JEDEC OUTLINE:
MS-026 BCE
MS-026 BCE-HD(THERMALLY ENHANCED VARIATIONS ONLY)
2.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS IMCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.



REVISION HISTORY

Version	Date	Revision	Page
Ver 1.0	10 Jul 2013	First release	