NT7963

DOT MATRIX LCD CONTROL LSI

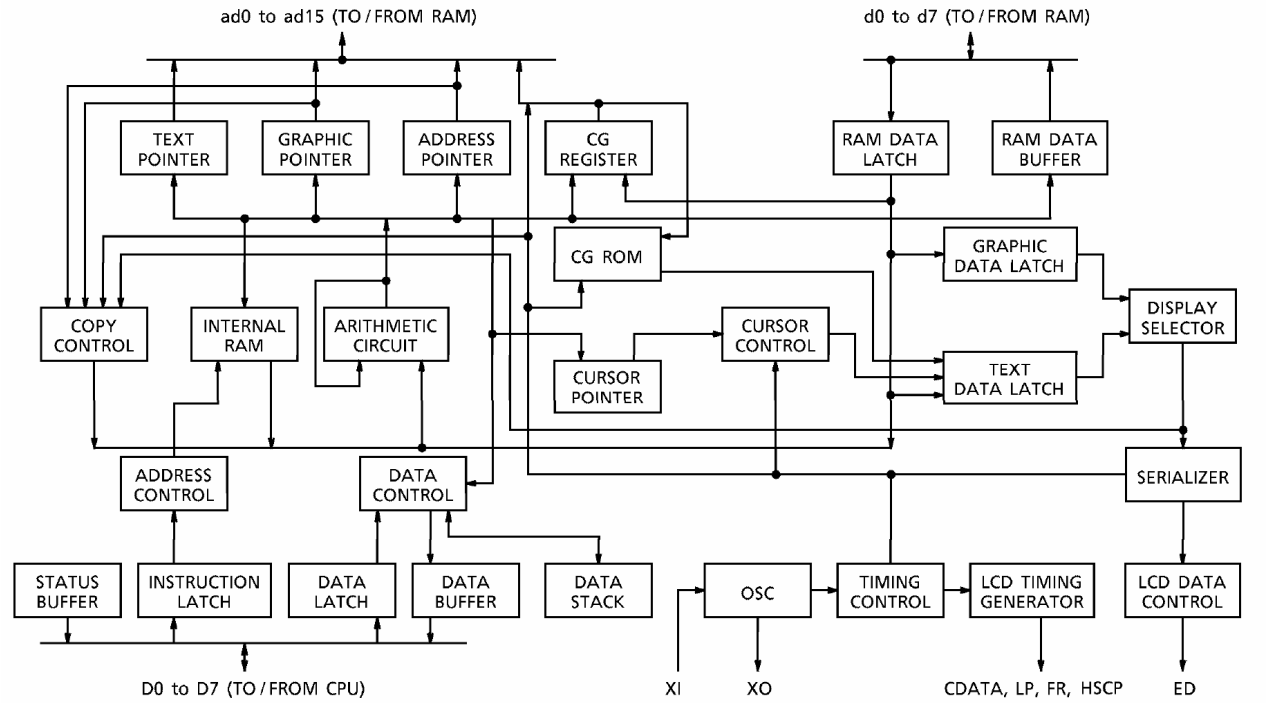
INTRODUCTION

The NT7963 is an LCD controller designed to be used with LCD control driver LSIs and data display memories. The device has an 8-bit parallel data bus and control lines for reading or writing through a MPU interface.
It has a 128 words character generator ROM which can control an external display RAM of up to 64 Kbytes. Allocation of text, graphic and external character generator RAM can be made easily and the display window can be moved freely within the allocated memory range.
The device supports a very board range of LCD formats be allowing selection of different combinations via set of programmable inputs. It can be used in text, graphic and combination text-and-graphic modes, and includes various attribute functions.

FEATURES

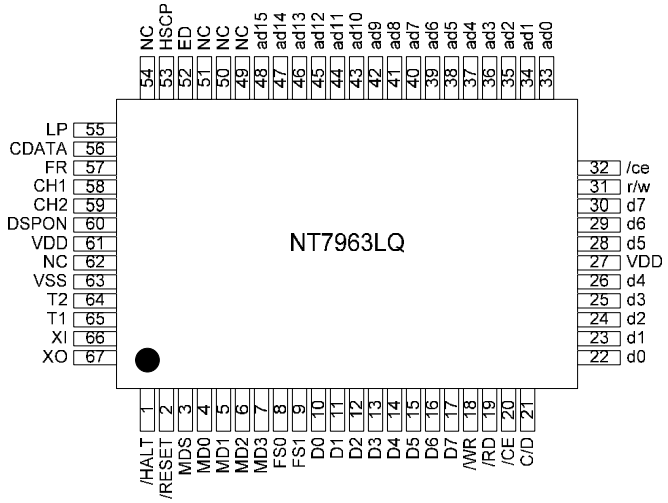
- Display format (pin-selectable)
  Columns: 32, 40, 64, 80
  Lines: 2, 4, 6, 8, 10, 12, 14, 16
  The combination of number of columns and number of lines must not cause the frequency to exceed 10 MHz.
- Character font (pin-selectable)
  Horizontal dots: 5, 6, 7, 8
  Vertical dots: 8 (fixed)
  It is necessary to set a character font in Graphic mode just as in Text mode. The oscillation frequency does not change with the font selection.
- Display duty: 1 / 16 to 1 / 128
- A 128−word character generator ROM is built in as standard.
- External display memory: 64 KB max
  The addresses in display memory of the text area, graphic area and external character generator area are determined by software.
- Read or Write operations from the CPU do not disturb the display.
- A crystal oscillator circuit is built in. The oscillation frequency is adjusted according to the display size. If using an external clock, use the XI pin as the clock input. (XO open.)
  External capacitors Crystal oscillation: 20 to 30 pF
  Ceramic oscillation: 30 to 100 pF
  Built in feedback resistor: 1MΩ (typ.)
- NT7086 can be connected to the device.
- External display RAM must be static RAM. The NT7963 cannot refresh D-RAM.
- The attribute functions can only be used in Text mode. They cannot be used in Graphic or Combination Character mode.

BLOCK DIAGRAM

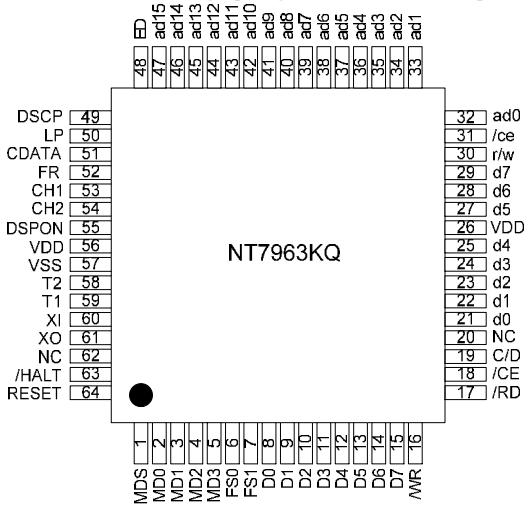


PIN ASSIGNMENT

NT7963LQ (LQFP-67L 14X20)



NT7963KQ (LQFP-64L 7X7)



ORDERING INFORMATION

Part No.	Remarks
NT7963LQ	LQFP-67L 14X20
NT7963KQ	LQFP-64L 7X7

PIN DESCRIPTION

<table>
<tr><th>PIN NAME</th><th>I/O</th><th>FUNCTIONS</th></tr>
<tr><td>MDS
MD0
MD1</td><td>Input</td><td>Pins for selection of LCD size
<table>
<tr><td>MDS</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td><td>H</td></tr>
<tr><td>MD1</td><td>H</td><td>H</td><td>L</td><td>L</td><td>H</td><td>H</td><td>L</td><td>L</td></tr>
<tr><td>MD0</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td></tr>
<tr><td>LINES</td><td>2</td><td>4</td><td>6</td><td>8</td><td>10</td><td>12</td><td>14</td><td>16</td></tr>
<tr><td>V-DOTS</td><td>16</td><td>32</td><td>48</td><td>64</td><td>80</td><td>96</td><td>112</td><td>128</td></tr>
<tr><td></td><td colspan="8">1 SCREEN</td></tr>
</table></td></tr>
<tr><td>MD2
MD3</td><td>Input</td><td>Pins for selection of number of columns
<table>
<tr><td>MD2</td><td>H</td><td>L</td><td>H</td><td>L</td></tr>
<tr><td>MD3</td><td>H</td><td>H</td><td>L</td><td>L</td></tr>
<tr><td>Columns</td><td>32</td><td>40</td><td>64</td><td>80</td></tr>
</table></td></tr>
<tr><td>FS0
FS1</td><td>Input</td><td>Pins for selection of font
<table>
<tr><td>FS0</td><td>H</td><td>L</td><td>H</td><td>L</td></tr>
<tr><td>FS1</td><td>H</td><td>H</td><td>L</td><td>L</td></tr>
<tr><td>Font</td><td>5 x 8</td><td>6 x 8</td><td>7 x 8</td><td>8 x 8</td></tr>
</table></td></tr>
<tr><td>D0 to D7</td><td>I/O</td><td>Data I/O pins between CPU and NT7963 (D7 is MSB)</td></tr>
<tr><td>/WR</td><td>Input</td><td>Data Write. Write data into NT7963 when /WR=L</td></tr>
<tr><td>/RD</td><td>Input</td><td>Data Read. Read data from NT7963 when /RD=L</td></tr>
<tr><td>/CE</td><td>Input</td><td>Chip Enable for NT7963. /CE must be L when CPU communicates with NT7963</td></tr>
<tr><td>C/D</td><td>Input</td><td>/WR=L …… C/D=H: Command Write C/D=L: Data Write
/RD=L …… C/D=H: Status Read C/D=L: Data Read</td></tr>
<tr><td>/HALT</td><td>Input</td><td>H …… Normal, L …… Stops the oscillation of the clock</td></tr>
<tr><td>/RESET</td><td>Input</td><td>H …… Normal (NT7963 has internal pull-up resistor)
L …… Initialize NT7963. Text and graphic have addresses and text and graphic area settings are retained</td></tr>
<tr><td>DSPON</td><td>Output</td><td>Control pin for external DC/DC. DSPON is L when /HALT is L or /RESET is L
(When DSPON goes H, the column drivers are cleared.)</td></tr>
<tr><td>/ce</td><td>Output</td><td>Chip enable pin for display memory</td></tr>
<tr><td>d0 to d7</td><td>I/O</td><td>Data I/O pins for display memory</td></tr>
<tr><td>ad0 to ad15</td><td>Output</td><td>Address outputs for display memory</td></tr>
<tr><td>r/w</td><td>Output</td><td>Read / Write signal for display memory</td></tr>
<tr><td>ED</td><td>Output</td><td>Data output for LCD</td></tr>
<tr><td>CDATA</td><td>Output</td><td>Synchronous signal for row driver</td></tr>
<tr><td>HSCP</td><td>Output</td><td>Shift clock pulse for LCD</td></tr>
<tr><td>LP</td><td>Output</td><td>Latch pulse for column driver. Shift clock pulse for row driver</td></tr>
<tr><td>FR</td><td>Output</td><td>Frame signal</td></tr>
<tr><td>XI</td><td>Input</td><td>Crystal oscillator input</td></tr>
<tr><td>XO</td><td>Output</td><td>Crystal oscillator output</td></tr>
<tr><td>CH1, CH2</td><td>Output</td><td>Check signal</td></tr>
<tr><td>/T1, /T2</td><td>Input</td><td>Test input. Usually Open, has internal Pull-up resistor</td></tr>
<tr><td>VDD</td><td>Power</td><td>Power supply (2.7~5.5V)</td></tr>
<tr><td>VSS</td><td>Power</td><td>Power supply (0V)</td></tr>
</table>

FUNCTION DEFINITION

- After power on, it is necessary to reset. /RESET is kept L between 5 clocks up (oscillation clock).
- When /HALT=L, the oscillation stops. The power supply for the LCD must now be turned off, to protect the LCD from DC bias.
- The HALT function includes the RESET function.
- The column / line counter and display register are cleared by /RESET. (Other registers are not cleared.) Disable the display using the clear-display register.
- The status must be checked before data or commands are sent. The MSB=0 status check must be done in particular. There is a possibility of erroneous operation due to a hard interrupt.
- STA0 and STA1 must be checked at the same time. When a command is executed, data transmission errors may occur.
- The NT7963 can only handle one byte per machine cycle (16 clocks). It is impossible to send more than two data in a machine cycle.
- When using a command with operand data, it is important to send the data first, and then execute the command.
- The character codes used by the NT7963 are different from ASCII codes.
- Status after RESET/HALT

TERMINAL	HALT	RESET
D0 to D7	F	F
d0 to d7	Final data	Final data
r/w	H	H
/ce	H (note 1)	H (note 1)
ad0 to ad15	H (note 2)	H (note 2)
ED	Final data	Final data
HSCP	L	L
LP	L	L
CDATA	H	H
FR	H	H
CH1	L	K0
CH2	L	VEND
DSPON	L	L
XO	H	OSC clock

H: Level H
L: Level L
F: Floating (high impedance)
K0: Test signal
VEND: Test signal
(Note 1): In Attribute mode, H or L according to status of graphic pointer
(Note 2): In Attribute mode, data of graphic pointer

- The relationship between number of row / column and oscillation clock

  The frequency of the crystal oscillator is adjusted by the following formula.

  f_{OSC} : Frequency of oscillation

  f_{SCP} : Frequency of shift clock ($f_{SCP} = f_{OSC} / 2$)

  f_R : Frequency of Frame

  M : Number of characters on one line (number of dots on one line=8M)

  For all font sizes (e.g. 7 × 8, 6 × 8, 5 × 8) the oscillation frequency remains constant.

  N : Number of rows (duty = 1 / 8N)

  $$\frac{8M}{f_{SCP}} \times 8N = \frac{1}{F_R}$$

  $f_{OSC} = f_R \times 64 \times 2 \times M \times N$

  (f_R = 60 Hz)

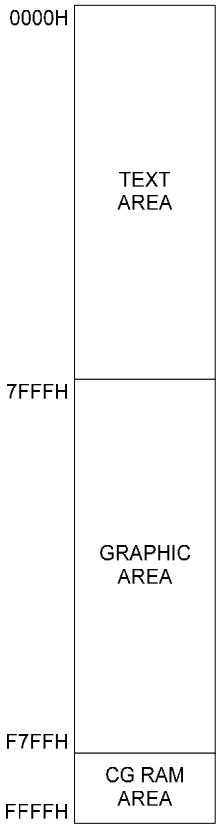
N \ M	32	40	64	80	duty
2	0.492	0.614	0.983	1.229	1/16
4	0.983	1.229	1.966	2.458	1/32
6	1.475	1.843	2.949	3.686	1/48
8	1.966	2.458	3.932	4.915	1/64
10	2.458	3.072	4.915	6.144	1/80
12	2.949	3.686	5.898	7.373	1/96
14	3.440	4.300	6.881	8.602	1/112
16	3.932	4.915	7.864	9.830	1/128

Unit: MHz

- RAM Interface

  The external RAM is used to store display data (text, graphic and external CG data). Text data, graphic data and external CG data can be freely allocated to the memory area (64 KB max).

  Example:



- Flowchart of communications with MPU

(1) Status Read

A status check must be performed before data is read or written.

Status check

The Status of NT7963 can be read from the data lines.

/RD L
/WR H
/CE L
C/D H
D0 to D7 Status word

The NT7963 status word format is as follows:

MSB							LSB
STA7 D7	STA6 D6	STA5 D5	STA4 D4	STA3 D3	STA2 D2	STA1 D1	STA0 D0

STA0	Check command execution capability	0: Disable 1: Enable
STA1	Check data read / write capability	0: Disable 1: Enable
STA2	Check auto mode data read capability	0: Disable 1: Enable
STA3	Check auto mode data write capability	0: Disable 1: Enable
STA4	Not used	
STA5	Check controller operation capability	0: Disable 1: Enable
STA6	Error flag. Used for screen peek and screen copy commands	0: No error 1: Error
STA7	Check the blank condition	0: Display off 1: Normal display

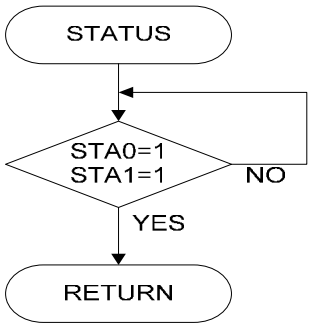
Note 1: It is necessary to check STA0 and STA1 at the same time.
There is a possibility of erroneous operation due to a hardware interrupt.

Note 2: For most modes STA0 / STA1 are used as a status check.

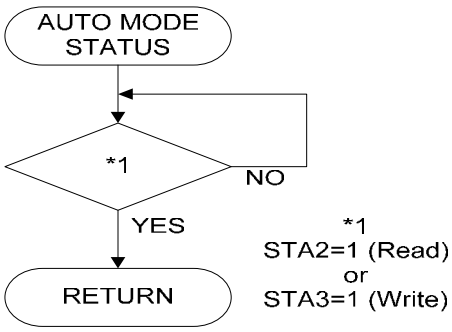
Note 3: STA2 and STA3 are valid in Auto mode; STA0 and STA1 are invalid.

Status checking flow

a)



b)



Note 4: When using the MSB = 0 command, a Status Read must be performed.

If a status check is not carried out, the NT7963 cannot operate normally, even after a delay time.

The hardware interrupt occurs during the address calculation period (at the end of each line).

If a MSB = 0 command is sent to the NT7963 during this period, the NT7963 enters Wait status.

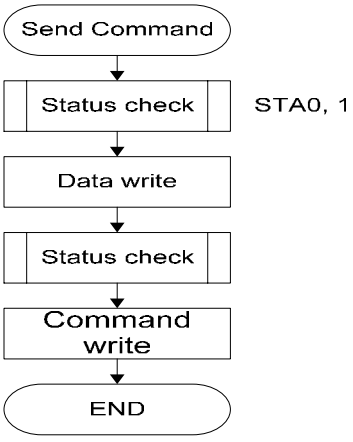
If a status check is not carried out in this state before the next command is sent, there is the possibility that the command or data will not be received.

(2) Setting data

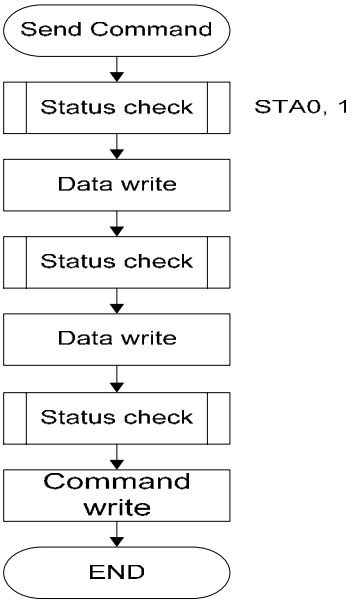
When using the NT7963, first set the data, then set the command.

Procedure for sending a command

a) The case of 1 data



b) The case of 2 data



Note: When sending more than two data, the last datum (or last two data) is valid.

COMMAND DEFINITION

COMMAND	CODE	D1	D2	FUNCTION
Register Setting	00100001	X address	Y address	Set Cursor Pointer
	00100010	Data	00H	Set Offset Register
	00100100	Low address	High address	Set Address Pointer
Set Control Word	01000000	Low address	High address	Set Text Home Address
	01000001	Columns	Columns	Set Text Area
	01000010	Low address	High address	Set Graphic Home Address
	01000011	Columns	Columns	Set Graphic Area
Mode Set	1000x000	-	-	OR Mode
	1000x001	-	-	EXOR Mode
	1000x011	-	-	AND Mode
	1000x100	-	-	Text Attribute Mode
	10000xxx	-	-	Internal CG ROM Mode
	10001xxx	-	-	External CG RAM Mode
Display Mode	10010000	-	-	Display off
	1001xx10	-	-	Cursor on, blink off
	1001xx11	-	-	Cursor on, blink on
	100101xx	-	-	Text on, graphic off
	100110xx	-	-	Text off, graphic on
	100111xx	-	-	Text on, graphic on
Cursor Pattern Select	10100000	-	-	1-line cursor
	10100001	-	-	2-line cursor
	10100010	-	-	3-line cursor
	10100011	-	-	4-line cursor
	10100100	-	-	5-line cursor
	10100101	-	-	6-line cursor
	10100110	-	-	7-line cursor
	10100111	-	-	8-line cursor
Data Auto Read/Write	10110000	-	-	Set Data Auto Write
	10110001	-	-	Set Data Auto Read
	10110010	-	-	Auto Reset
Data Read/Write	11000000	Data	-	Data Write and Increase ADP
	11000001	-	-	Data Read and Increase ADP
	11000010	Data	-	Data Write and Decrease ADP
	11000011	-	-	Data Read and Decrease ADP
	11000100	Data	-	Data Write and Non-variable ADP
	11000101	-	-	Data Read and Non-variable ADP
Screen peek	11100000	-	-	Screen Peek
Screen copy	11101000	-	-	Screen Copy

COMMAND	CODE	D1	D2	FUNCTION
Bit Set/Reset	11110xxx	-	-	Bit Reset
	11111xxx	-	-	Bit Set
	1111x000	-	-	Bit 0 (LSB)
	1111x001	-	-	Bit 1
	1111x010	-	-	Bit 2
	1111x011	-	-	Bit 3
	1111x100	-	-	Bit 4
	1111x101	-	-	Bit 5
	1111x110	-	-	Bit 6
	1111x111	-	-	Bit 7 (MSB)

- Setting register

CODE	HEX.	FUNCTION	D1	D2
00100001	21H	Set Cursor Pointer	X address	Y address
00100010	22H	Set Offset Register	Data	00H
00100100	24H	Set Address Pointer	Low address	High address

(1) Set Cursor Pointer

The position of the cursor is specified by X Address and Y Address. The cursor position can only be moved by this command. Data read / write from the MPU never changes the cursor pointer.

X Address and Y Address are specified as follows.

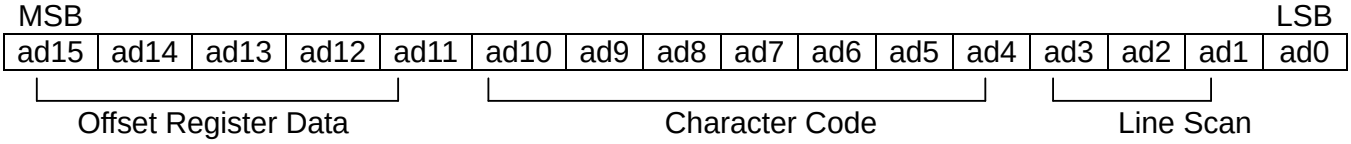
X Address 00H to 4FH (lower 7 bits are valid)

Y Address 00H to 0FH (lower 4 bits are valid)

(2) Set Offset Register

The offset register is used to determine the external character generator RAM area.

The NT7963 has a 16−bit address bus as follows:



NT7963 assign external character generator, when character code set 80H to FFH in using internal character generator. Character code 00H to FFH assign external character generator, when external generator mode.

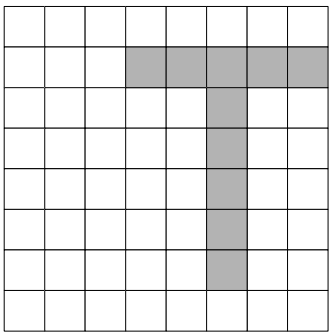
The senior five bits define the start address in external memory of the CG RAM area. The next eight bits represent the character code of the character. In internal CG ROM mode, character codes 00H to 7FH represent the predefined “internal” CG ROM characters, and codes 80H to FFH represent the user’s own “external” characters. In external CG RAM mode, all 256 codes from 00H to FFH can be used to represent the user's own characters. The three least significant bits indicate one of the eight rows of eight dots that define the character’s shape.

The relationship between display RAM address and offset register

Offset register data	CG RAM hex. address (start to end)
00000	0000 to 07FFH
00001	0800 to 0FFFH
00010	1000 to 17FFH
11100	E000 to E7FFH
11101	E800 to EFFFH
11110	F000 to F7FFH
11111	F800 to FFFFH

(Example 1)

Offset register	02H				
Character code	80H				
Character generator RAM start address	0001	0100	0000	0000	
	1	4	0	0	H



(address)	(data)
1400H	00H
1401H	1FH
1402H	04H
1403H	04H
1404H	04H
1405H	04H
1406H	04H
1407H	00H

(Example 2) The relationship between display RAM data and display characters

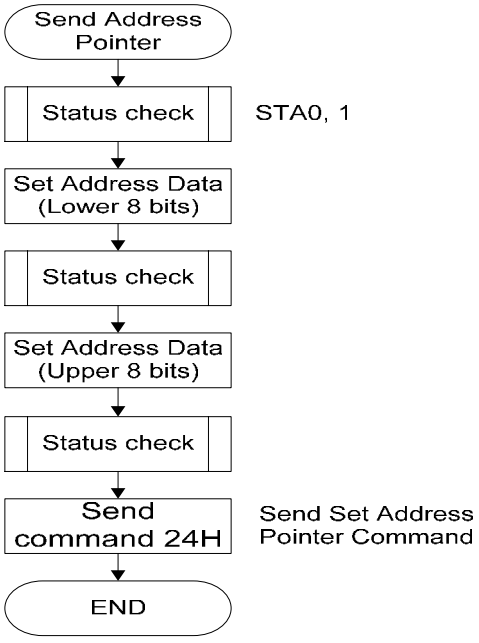
Display character	(RAM data)	(Character)
AB γ DEζGHIJKLM	21H	A
	22H	B
	83H	γ
	24H	D
	25H	E
	86H	ζ

γ and ζ are displayed by character generator RAM.

(3) Set Address Pointer

The Set Address Pointer command is used to indicate the start address for writing to (or reading from) external RAM.

The Flowchart for Set Address Pointer command



- Set Control Word

CODE	HEX.	FUNCTION	D1	D2
01000000	40H	Set Text Home Address	Low address	High address
01000001	41H	Set Text Area	Columns	00H
01000010	42H	Set Graphic Home Address	Low address	High address
01000011	43H	Set Graphic Area	Columns	00H

The home address and column size are defined by this command

(1) Set Text Home Address

The starting address in the external display RAM for text display is defined by this command. The text home address indicates the leftmost and uppermost position.

The relationship between external display RAM address and display position.

TH		TH+CL
TH+TA		TH+TA+CL
(TH+TA)+TA		TH+2TA+CL
(TH+2TA)+TA		TH+3TA+CL
TH+(n-1) TA		TH+(n-1) TA+CL

TH: Text home address
TA: Text area number (columns)
CL: Columns are fixed by hardware (pin-programmable).

(Example)

Text home address	: 0000H
Text area	: 0020H
MD2 = H, MD3 = H	: 32 columns
MDS = L, MD0 = L, MD1 = H	: 4 lines

0000H	0001H		001EH	001FH
0020H	0021H		003EH	003FH
0040H	0041H		005EH	005FH
0060H	0061H		007EH	007FH

(2) Set Graphic Home Address

The starting address in the external display RAM used for graphic display is defined by this command. The graphic home address indicates the leftmost and uppermost position.

The relationship between external display RAM address and display position.

GH		GH+CL
GH+GA		GH+GA+CL
(GH+GA)+GA		GH+2GA+CL
(GH+2GA)+GA		GH+3GA+CL
GH+(n-1) GA		GH+(n-1) GA+CL

GH: Graphic home address
GA: Graphic area number (columns)
CL: Columns are fixed by hardware (pin-programmable).

(Example)

Graphic home address	: 0000H
Graphic area	: 0020H
MD2 = H, MD3 = H	: 32 columns
MDS = L, MD0 = H, MD1 = H	: 2 lines

0000H	0001H		001EH	001FH
0020H	0021H		003EH	003FH
0040H	0041H		005EH	005FH
0060H	0061H		007EH	007FH
0080H	0081H		009EH	009FH
00A0H	00A1H		00BEH	00BFH
00C0H	00C1H		00DEH	00DFH
00E0H	00E1H		00FEH	00FFH
0100H	0101H		011EH	011FH
0120H	0121H		013EH	013FH
0140H	0141H		015EH	015FH
0160H	0161H		017EH	017FH
0180H	0181H		019EH	019FH
01A0H	01A1H		01BEH	01BFH
01C0H	01C1H		01DEH	01DFH
01E0H	01E1H		01FEH	01FFH

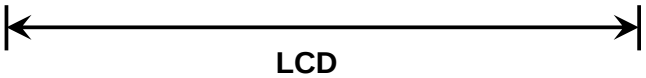
(3) Set Text Area

The display columns are defined by the hardware setting. This command can be used to adjust the columns of display.

(Example)

LCD size	: 20 Columns, 4 lines
Text home address	: 0000H
Text area	: 0014H
MD2 = H, MD3 = H	: 32 columns
MDS = L, MD0 = L, MD1 = H	: 4 lines

0000H	0001H		0013H	0014H		001FH
0014H	0015H		0027H	0028H		0033H
0028H	0029H		003BH	003CH		0047H
003CH	003DH		004FH	0050H		005BH



LCD

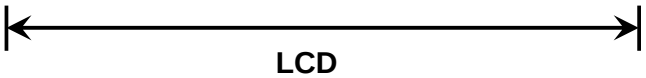
(4) Set Graphic Area

The display columns are defined by the hardware setting. This command can be used to adjust the columns of the graphic display.

(Example)

LCD size	: 20 Columns, 2 lines
Graphic home address	: 0000H
Graphic area	: 0014H
MD2 = H, MD3 = H	: 32 columns
MDS = L, MD0 = H, MD1 = H	: 2 lines

0000H	0001H		0013H	0014H		001FH
0014H	0015H		0027H	0028H		0033H
0028H	0029H		003BH	003CH		0047H
003CH	003DH		004FH	0050H		005BH
0050H	0051H		0063H	0064H		006FH
0064H	0065H		0077H	0078H		0083H
0078H	0079H		008BH	008CH		0097H
008CH	008DH		009FH	00A0H		00ABH
00A0H	00A1H		00B3H	00B4H		00BFH
00B4H	00B5H		00C7H	00C8H		00D3H
00C8H	00C9H		00DBH	00DCH		00E7H
00DCH	00DDH		00EFH	00F0H		00FDH
00F0H	00F1H		0103H	0104H		011FH
0104H	0105H		0117H	0118H		0123H
0118H	0119H		012BH	012CH		0137H
012CH	012DH		013FH	0140H		014BH



LCD

If the graphic area setting is set to match the desired number of columns on the LCD, the addressing scheme will be automatically modified so that the start address of each line equals the end address of the previous line + 1.

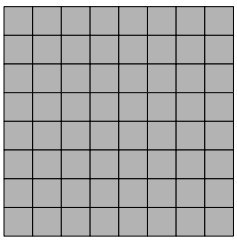
- Mode Set

CODE	FUNCTION	OPERAND
1000x000	OR Mode	-
1000x001	EXOR Mode	-
1000x011	AND Mode	-
1000x100	Text Attribute Mode	-
10000xxx	Internal Character Generator Mode	-
10001xxx	External Character Generator Mode	-

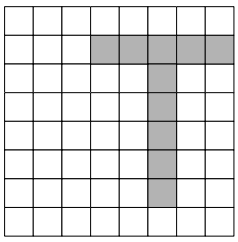
x: invalid

The display mode is defined by this command. The display mode does not change until the next command is sent. The logical OR, EXOR, AND of text or graphic display can be displayed.
In Internal Character Generator mode, character codes 00H to 7FH are assigned to the built-in character generator ROM. The character codes 80H to FFH are automatically assigned to the external character generator RAM.

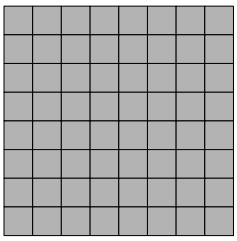
(Example)



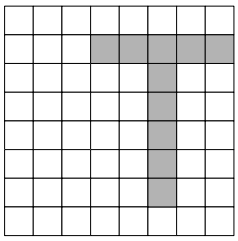
GRAPHIC



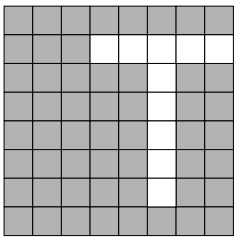
TEXT



“OR”



“AND”



“EXOR”

Note: Attribute functions can only be applied to text display, since the attribute data is placed in the graphic RAM area.

Attribute function

The attribute operations are Reverse display, Character blink and Inhibit. The attribute data is written into the graphic area which was defined by the Set Control Word command. Only text display is possible in Attribute Function mode; graphic display is automatically disabled. However, the Display Mode command must be used to turn both Text and Graphic on in order for the Attribute function to be available.

The attribute data for each character in the text area is written to the same address in the graphic area. The Attribute function is defined as follows.

Attribute RAM 1 byte

x	x	x	x	d3	d2	d1	d0

d3	d2	d1	d0	FUNCTION
0	0	0	0	Normal display
0	1	0	1	Reverse display
0	0	1	1	Inhibit display
1	0	0	0	Blink of normal display
1	1	0	1	Blink of reverse display
1	0	1	1	Blink of inhibit display

- Display mode

CODE	FUNCTION	OPERAND
10010000	Display off	-
1001xx10	Cursor on, blink off	-
1001xx11	Cursor on, blink on	-
100101xx	Text on, graphic off	-
100110xx	Text off, graphic on	-
100111xx	Text on, graphic on	-

x: invalid

1	0	0	1	D3	D2	D1	D0

D0 — Cursor blink — on: 1, off: 0
D1 — Cursor display — on: 1, off: 0
D2 — Text display — on: 1, off: 0
D3 — Graphic display — on: 1, off: 0

Note: It is necessary to turn on “Text display” and “Graphic display” in the following cases.

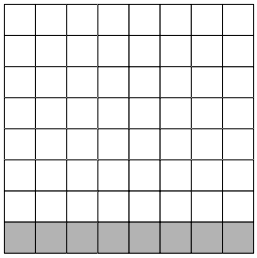
a) Combination of text / graphic display

b) Attribute function

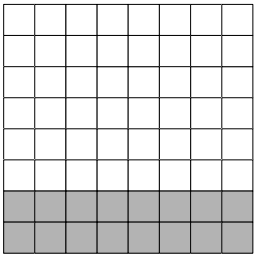
- Cursor pattern select

CODE	FUNCTION	OPERAND
10100000	1- line cursor	-
10100001	2- line cursor	-
10100010	3- line cursor	-
10100011	4- line cursor	-
10100100	5- line cursor	-
10100101	6- line cursor	-
10100110	7- line cursor	-
10100111	8- line cursor	-

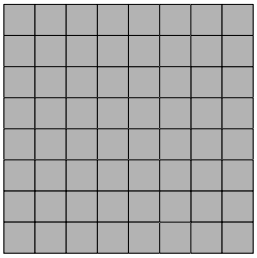
When cursor display is ON, this command selects the cursor pattern in the range 1 line to 8 lines. The cursor address is defined by the Cursor Pointer Set command.



1-line cursor



2-line cursor



8-line cursor

- Data Auto Read/Write

CODE	HEX.	FUNCTION	OPERAND
10110000	B0H	Set Data Auto Write	-
10110001	B1H	Set Data Auto Read	-
10110010	B2H	Auto Reset	-

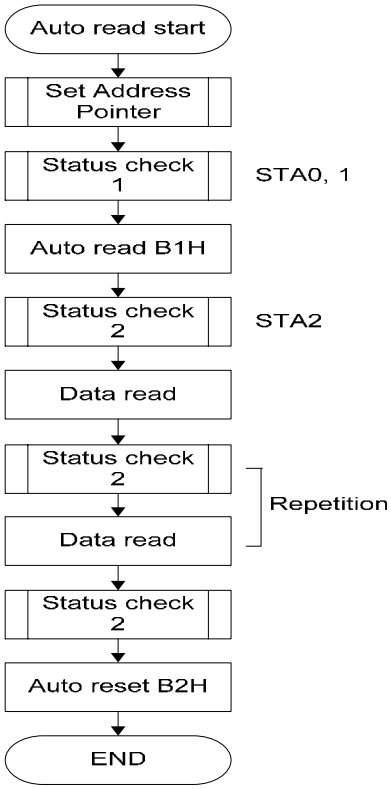
This command is convenient for sending a full screen of data from the external display RAM. After setting Auto mode, a Data Write (or Read) command is need not be sent between each datum. A Data Auto Write (or Read) command must be sent after a Set Address Pointer command. After this command, the address pointer is automatically incremented by 1 after each datum. In Auto mode, the NT7963 cannot accept any other commands.

The Auto Reset command must be sent to the NT7963 after all data has been sent, to clear Auto mode.

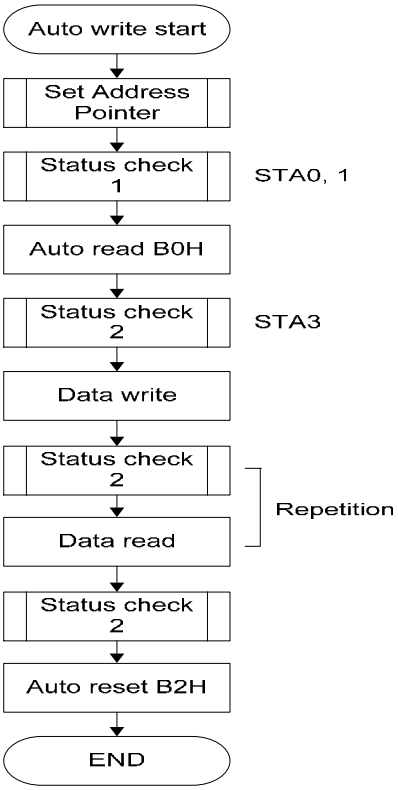
Note: A Status check for Auto mode

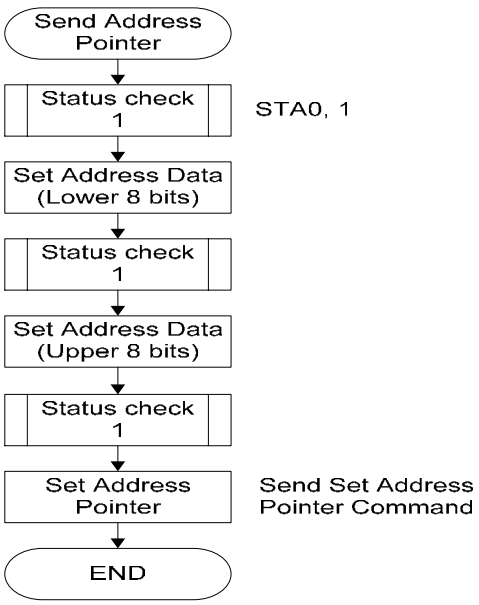
(STA2, STA3 should be checked between sending of each datum. Auto Reset should be performed after checking STA3 = 1 (STA2 = 1). Refer to the following flowchart.

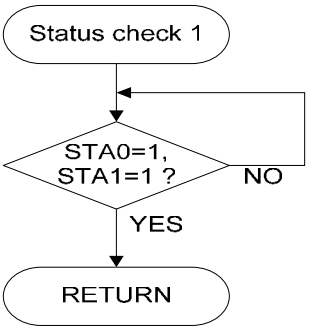
a)Auto Read Mode

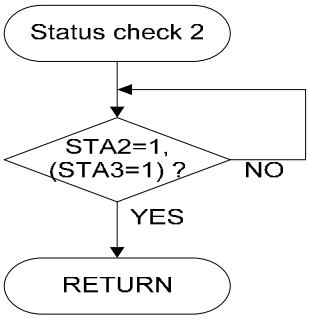


b) Auto Write mode







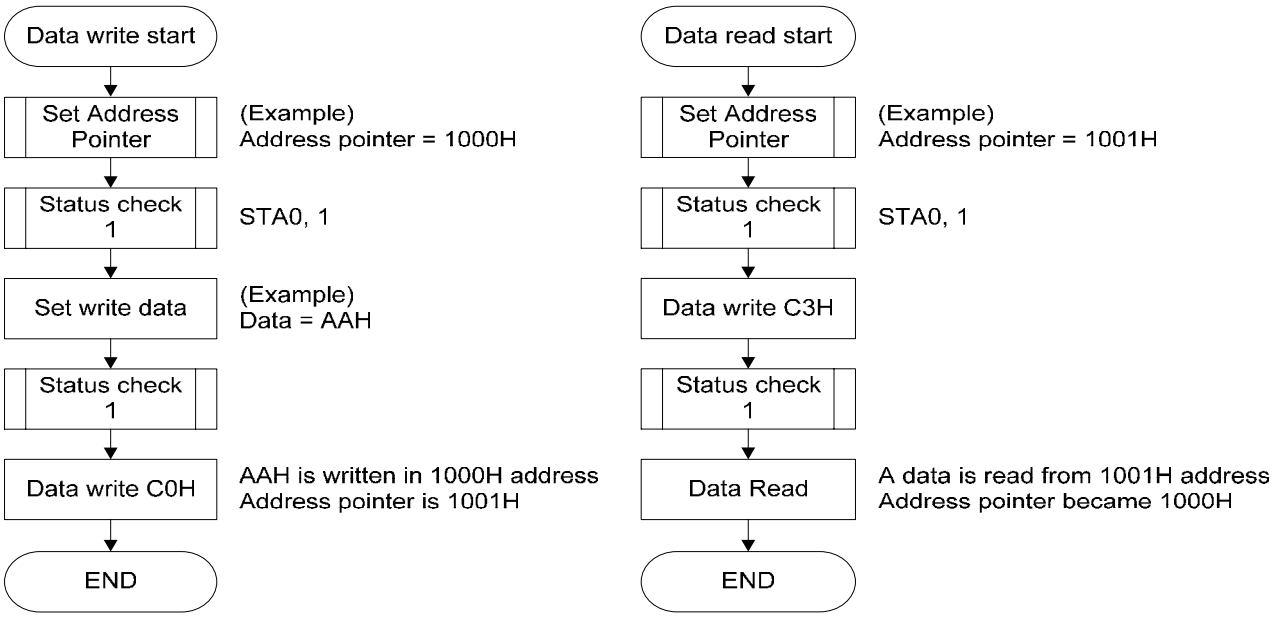


I Data Read/Write

CODE	HEX.	FUNCTION	OPERAND
11000000	C0H	Data Write and Increment ADP	Data
11000001	C1H	Data Read and Increment ADP	-
11000010	C2H	Data Write and Decrement ADP	Data
11000011	C3H	Data Read and Decrement ADP	-
11000100	C4H	Data Write and Non-variable ADP	Data
11000101	C5H	Data Read and Non-variable ADP	-

This command is used for writing data from the MPU to external display RAM, and reading data from external display RAM to the MPU. Data Write / Data Read should be executed after setting address using Set Address Pointer command. The address pointer can be automatically incremented or decremented using this command.

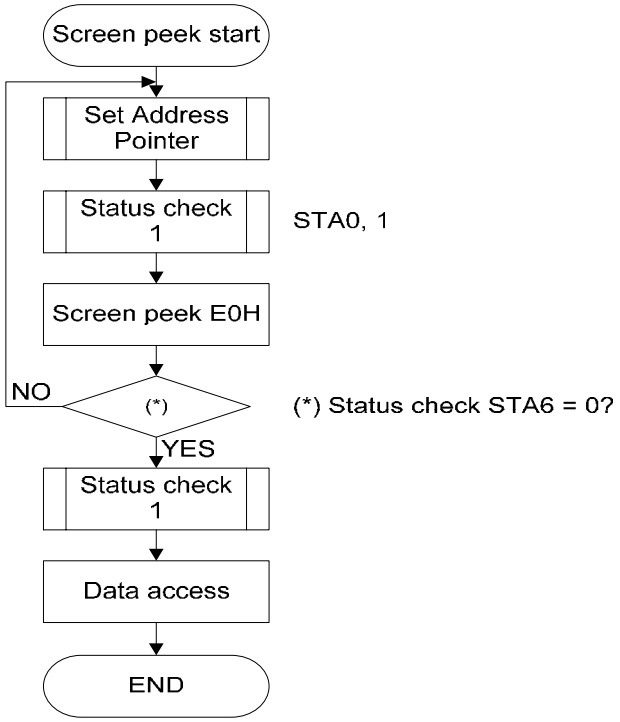
(Note) This command is necessary for each 1−byte datum. Refer to the following flowchart.



I Screen Peek

CODE	HEX.	FUNCTION	OPERAND
11100000	E0H	Screen Peek	-

This command is used to transfer 1 byte of displayed data to the data stack; this byte can then be read from the MPU by data access. The logical combination of text and graphic display data on the LCD screen can be read by this command.
The status (STA6) should be checked just after the Screen Peek command. If the address determined by the Set Address Pointer command is not in the graphic area, this command is ignored and a status flag (STA6) is set.
Refer to the following flowchart.

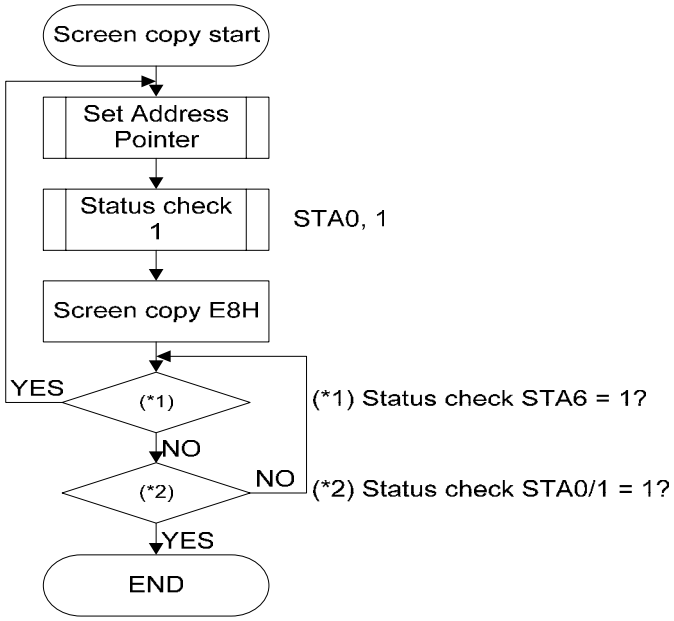


(Note) This command is available when hardware column number and software column number are the same. Hardware column number is related to MD2 and MD3 setting. Software column number is related to Set Text Area and Set Graphic Area command.

I Screen Copy

CODE	HEX.	FUNCTION	OPERAND
11101000	E8H	Screen Copy	-

This command copies a single raster line of data to the graphic area.
The start point must be set using the Set Address Pointer command.
(Note) If the attribute function is being used, this command is not available.
(With Attribute data is graphic area data.)
Refer to the following flowchart.



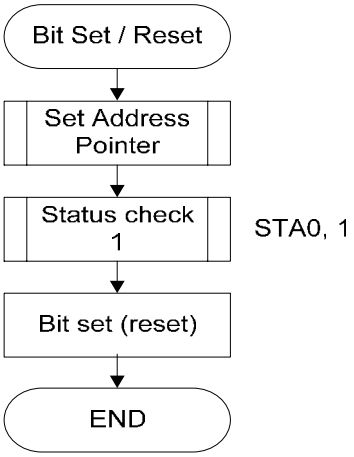
(Note) This command is available when hardware column number and software column number are the same. Hardware column number is related to MD2 and MD3 setting. Software column number is related to Set Text Area and Set Graphic Area command.

Bit Set/Reset

CODE	FUNCTION	OPERAND
11110xxx	Bit Reset	-
11111xxx	Bit Set	-
1111x000	Bit 0 (LSB)	-
1111x001	Bit 1	-
1111x010	Bit 2	-
1111x011	Bit 3	-
1111x100	Bit 4	-
1111x101	Bit 5	-
1111x110	Bit 6	-
1111x111	Bit 7 (MSB)	-

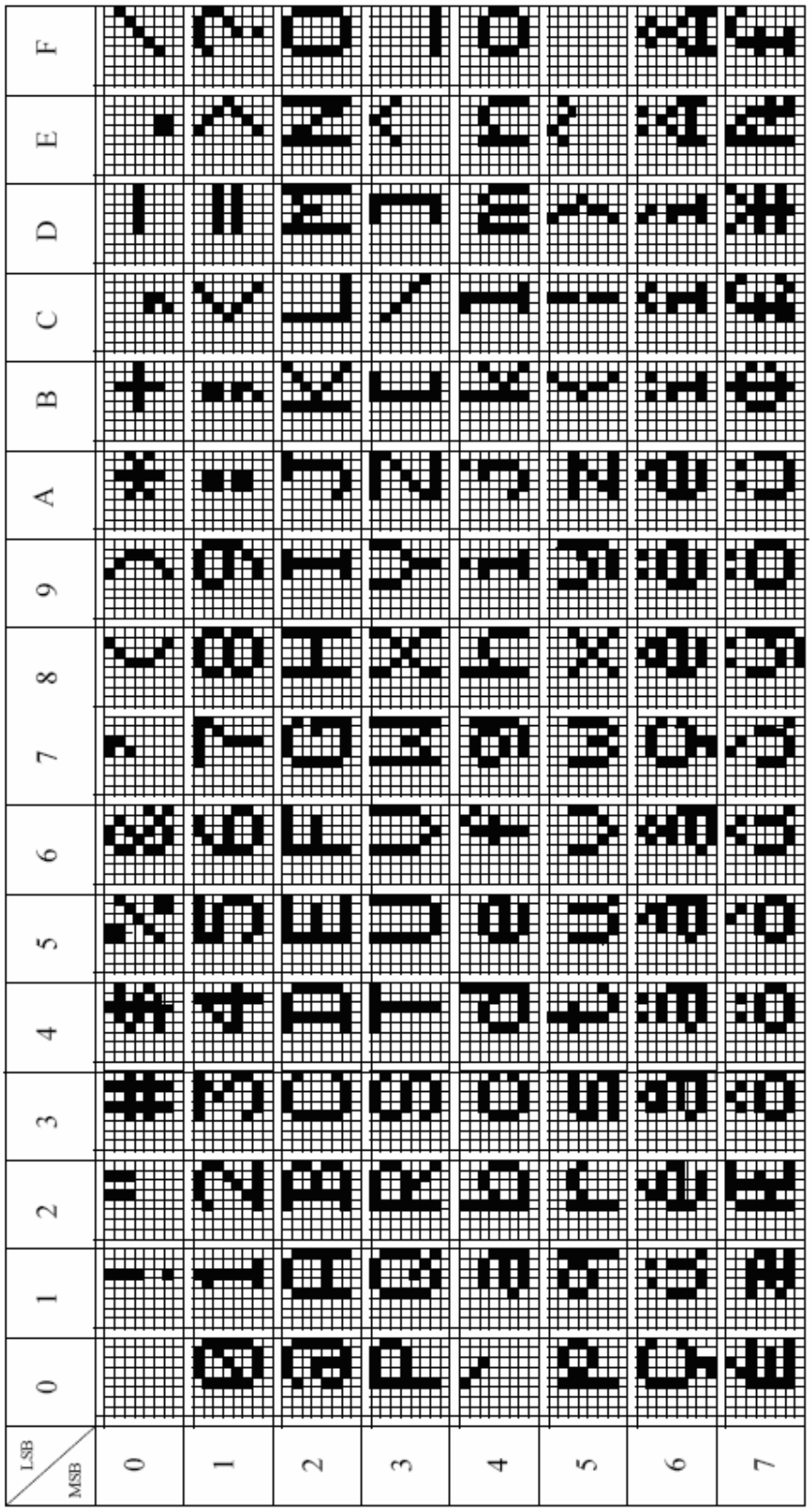
x: invalid

This command use to set or reset a bit of the byte specified by the address pointer. Only one bit can be set / reset at a time.
Refer to the following flowchart.



Character Code Map

The relation between character codes and character pattern



ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD} (Note)	-0.3 to 7.0	V
Input Voltage	V_{IN} (Note)	-0.3 to V_{DD}+0.3	V
Operating Temperature	Topr	-20 to 70	℃
Storage Temperature	Tstg	-55 to 125	℃

(Note) Referenced to V_{SS} = 0V

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

TEST CONDITION (Unless otherwise noted. V_{SS}=0V, V_{DD}=5.0V±10%, Ta= -20 to 75℃)

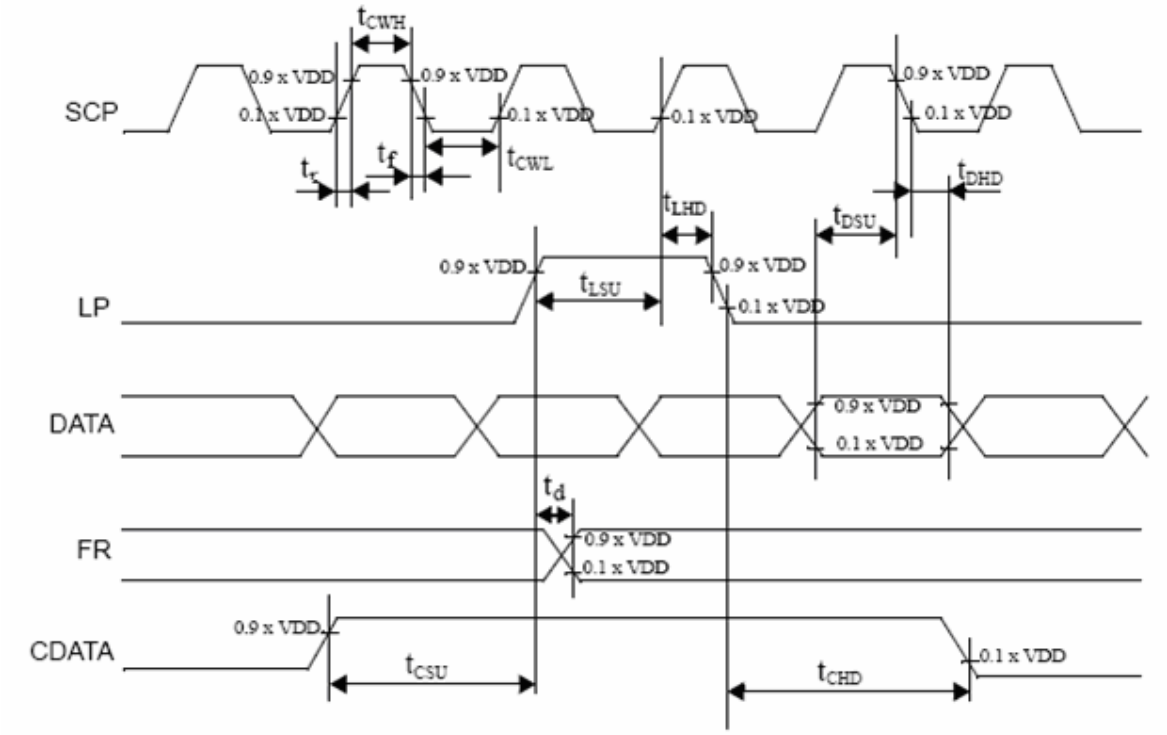
ITEM		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	PIN NAME
Operating Voltage		V_{DD}	-	2.7	5.0	5.5	V	V_{DD}
Input	H Level	V_{IH}	-	0.7V_{DD}	-	V_{DD}	V	Input pins
	L Level	V_{IL}	-	0	-	0.3V_{DD}	V	Input pins
Output Voltage	H Level	V_{OH}	-	V_{DD}-0.3	-	V_{DD}	V	Output pins
	L Level	V_{OL}	-	0	-	0.3	V	Output pins
Output Resistance	H Level	R_{OH}	V_{OUT}= VDD-0.5V	-	-	400	Ω	Output pins
	L Level	R_{OL}	V_{OUT}= 0.5V	-	-	400	Ω	Output pins
Input Pull-up resistance		R_{PU}	-	50	100	200	KΩ	(Note 1)
Operating Frequency		f_{OSC}	-	0.4	-	10	MHz	XI, XO
Current Consumption (Operating)		$I_{DD\ (1)}$	V_{DD}=5.0V (Note 2) f_{OSC}=3MHz	-	3.3	6	mA	V_{DD}
Current Consumption (Halt)		$I_{DD\ (2)}$	V_{DD}=5.0V	-	-	3	μA	V_{DD}

Note 1: Applied /RESET, T1, T2

Note 2: MDS = L, MD0 = L, MD1 = L, MD2 = H, MD3 = H, FS0 = L, FS1 = L, D7 to D0 = LHLHLHLH

AC CHARACTERISTICS

I Switching Characteristics (1)

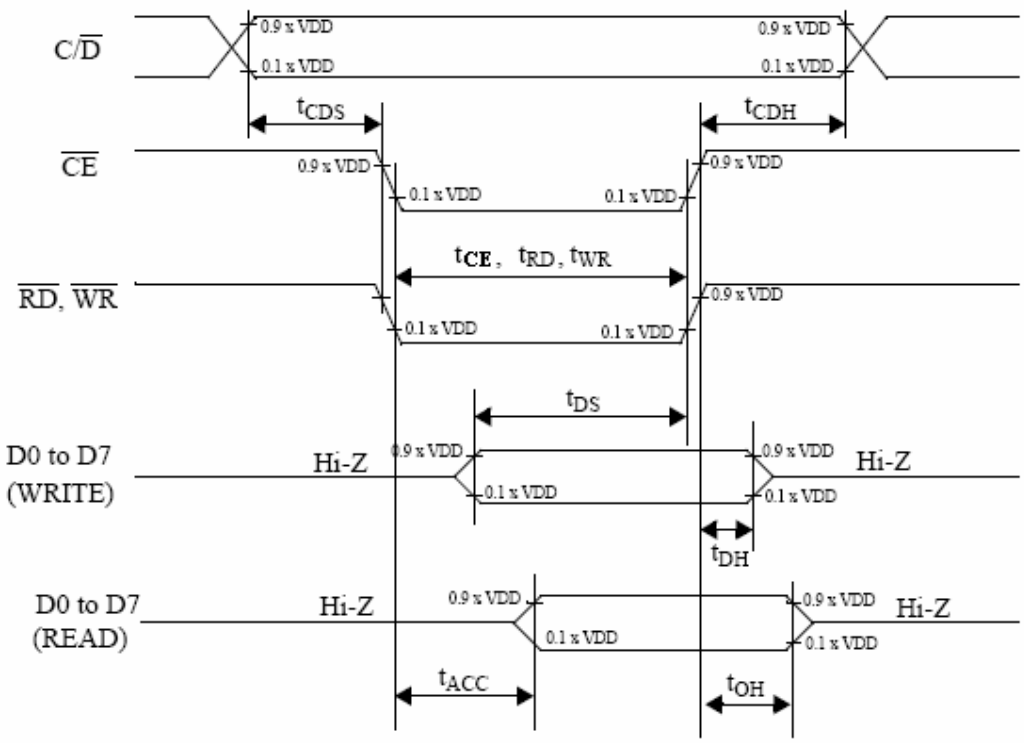


TEST CONDITION (Unless otherwise noted. V_{SS}=0V, V_{DD}=5.0V±10%, Ta= -20 to 75℃)

ITEM	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Operating Frequency	f_{scp}	Ta= -10~70℃	-	5.0	MHz
SCP Pulse Width	t_{CWH}, t_{CWL}	-	150	-	ns
SCP Rise / Fall Time	tr, tf	-	-	30	ns
LP Set-up Time	t_{LSU}	-	150	290	ns
LP Hold Time	t_{LHD}	-	5	40	ns
Data Set-up Time	t_{DSU}	-	170	-	ns
Data Hold Time	t_{DHD}	-	80	-	ns
FR Delay Time	t_d	-	0	90	ns
CDATA Set-up Time	t_{CSU}	-	450	850	ns
CDATA Hold Time	t_{CHD}	-	450	950	ns

I Switching Characteristics (2)

Bus Timing

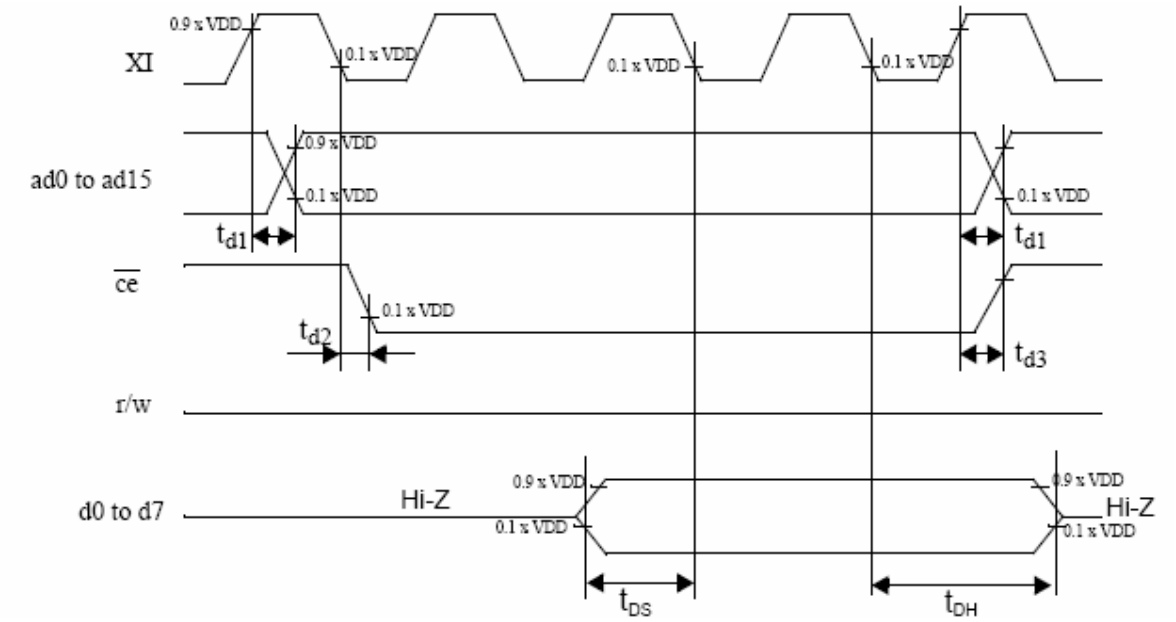


TEST CONDITION (Unless otherwise noted. V_{SS}=0V, V_{DD}=5.0V±10%, Ta= -20 to 75℃)

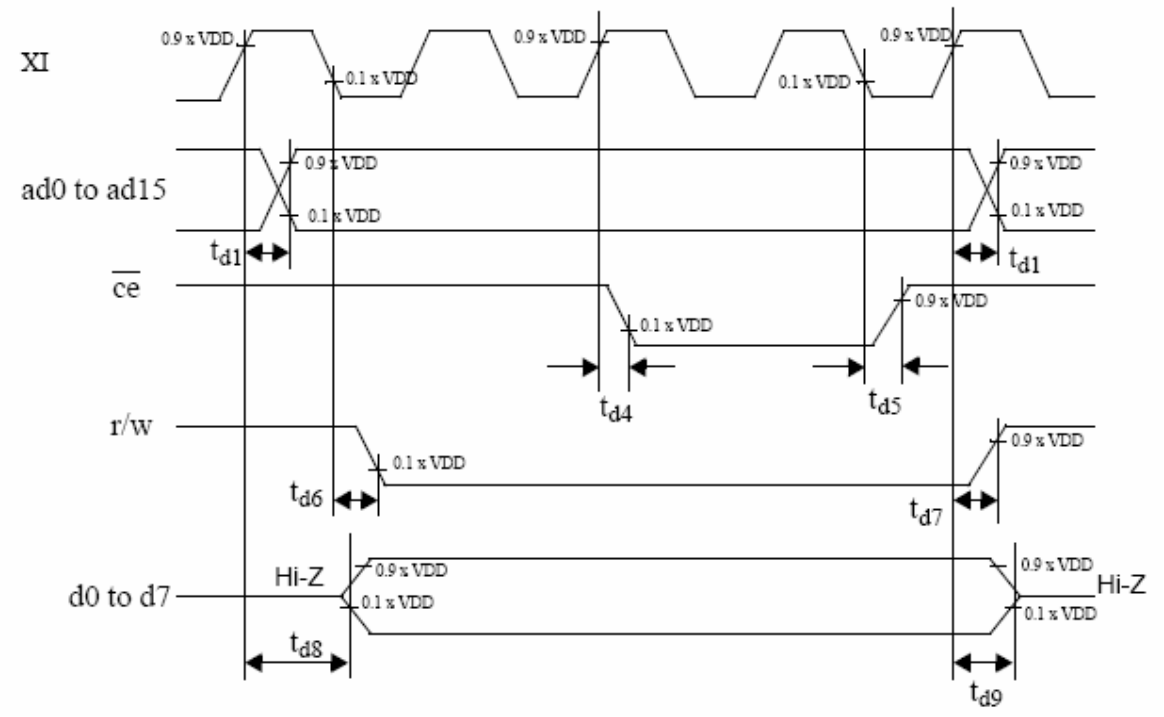
ITEM	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
C/D Set-up Time	t_{CDS}	-	100	-	ns
C/D Hold Time	t_{CDH}	-	10	-	ns
/CE, /RD, /WR, Pulse Width	t_{CE}, t_{RD}, t_{WR}	-	80	-	ns
Data Set-up Time	t_{DS}	-	80	-	ns
Data Hold Time	t_{DH}	-	40	-	ns
Access Time	t_{ACC}	-	-	150	ns
Output Hold Time	t_{OH}	-	10	50	ns

I Switching Characteristics (3)

(1) External RAM Read mode



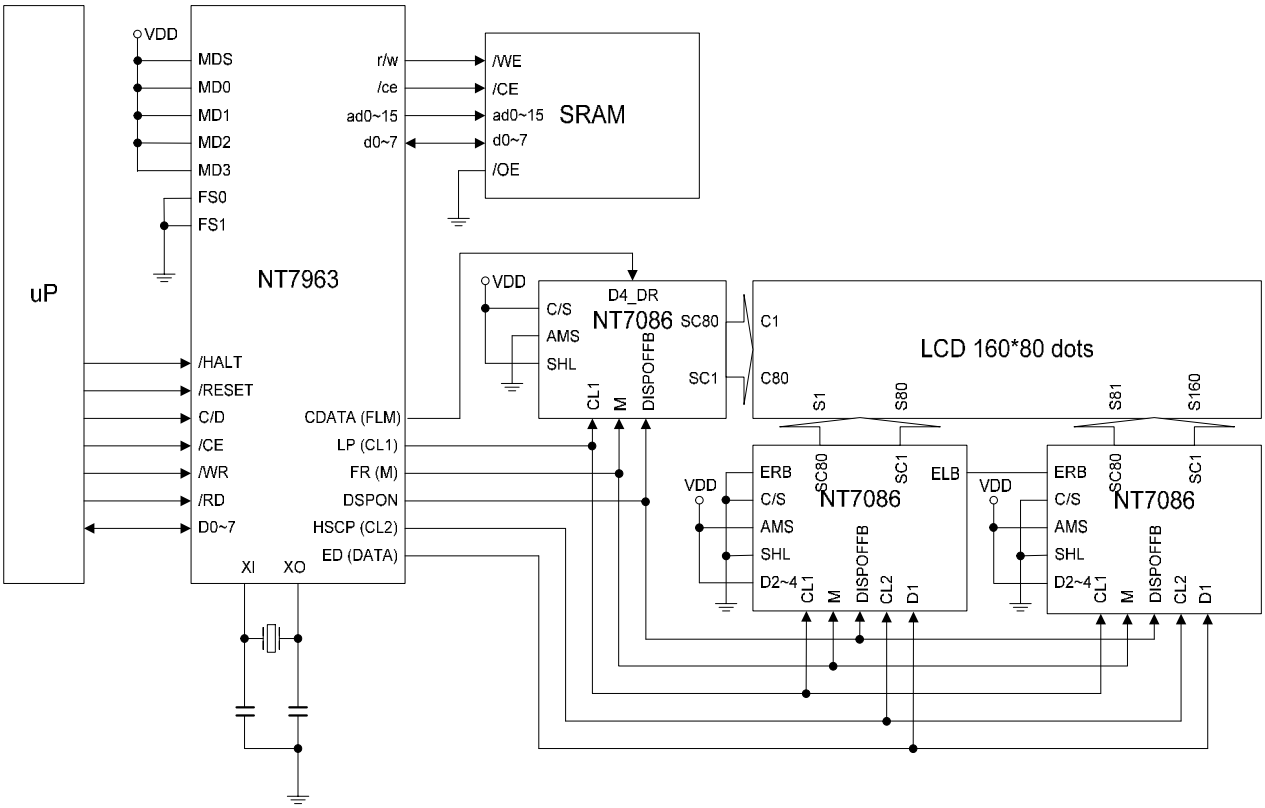
(2) External RAM Write mode



TEST CONDITION (Unless otherwise noted. V_{SS}=0V, V_{DD}=5.0V±10%, Ta= -20 to 75℃)

ITEM	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Address Delay Time	t_{d1}	-	-	250	ns
/ce Fall Delay Time (Read)	t_{d2}	-	-	180	ns
/ce Rise Delay Time (Read)	t_{d3}	-	-	180	ns
Data Set-up Time	t_{DS}	-	0	-	ns
Data Hold Time	t_{DH}	-	30	-	ns
/ce Fall Delay Time (Write)	t_{d4}	-	-	200	ns
/ce Rise Delay Time (Write)	t_{d5}	-	-	200	ns
r/w Fall Delay Time	t_{d6}		-	180	ns
r/w Rise Delay Time	t_{d7}		-	180	ns
Data Stable Time	t_{d8}		-	450	ns
Data Hold Time	t_{d9}		-	200	ns

APPLICATION CIRCUIT



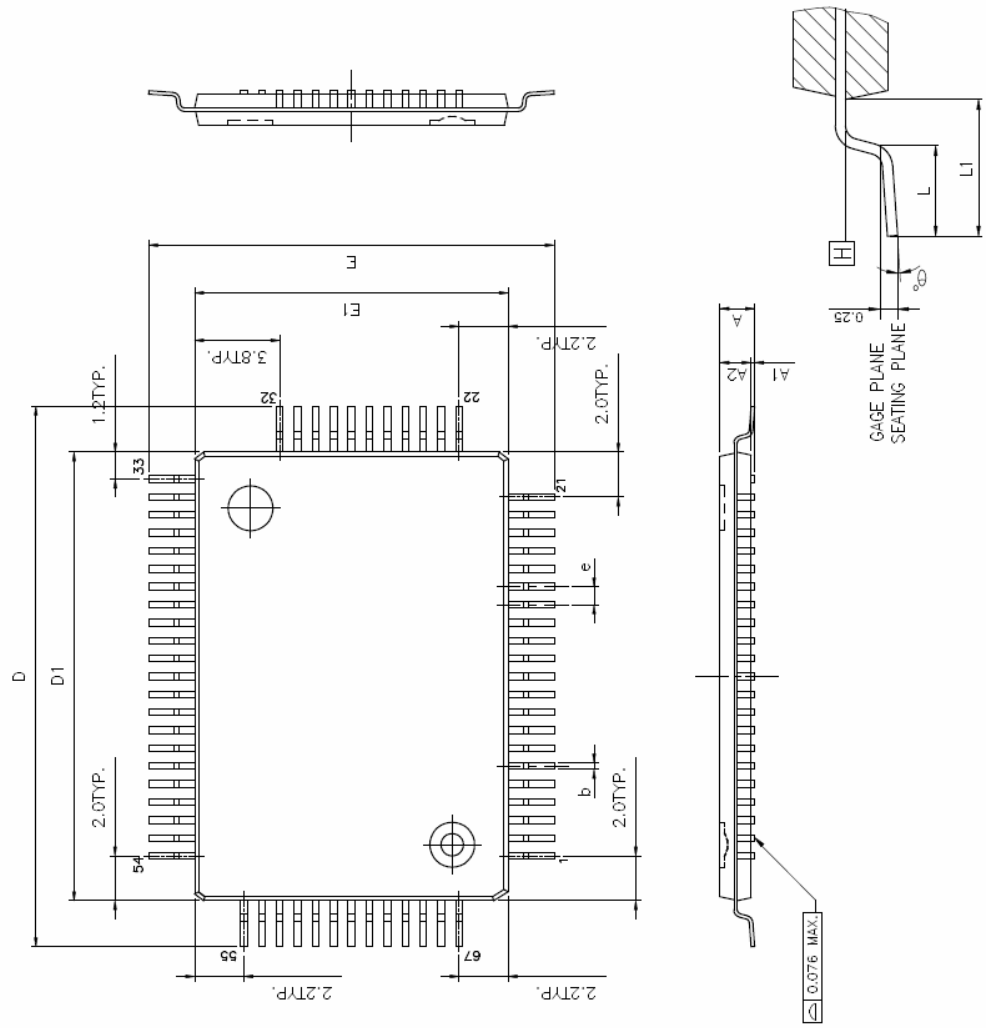
OUTLINE DRAWING (LQFP-67L 14X20)

SYMBOLS	MIN.	NOM	MAX.
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
b	0.20	0.30	0.40
D		24.10 BASIC	
D1		20.00 BASIC	
e		0.8 BASIC	
E		18.10 BASIC	
E1		14.00 BASIC	
L	1.15	1.35	1.55
L1		2.05 REF.	
θ°	0	3.5	7

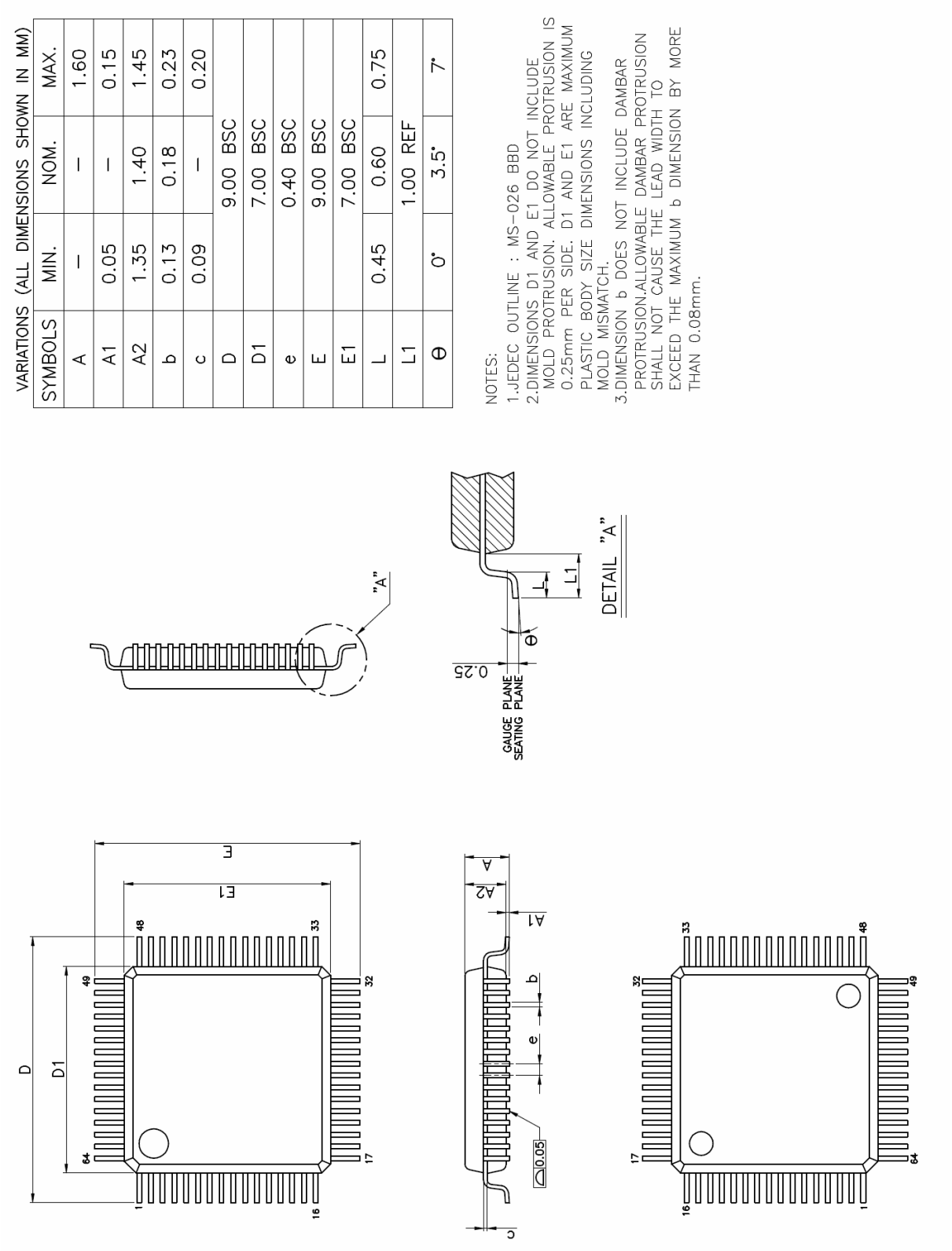
△3

UNIT : mm

NOTES:
1.JEDEC : N/A.
2.DATUM PLANE [H] IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [H].
4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION .



OUTLINE DRAWING (LQFP-64L 7X7)



NT7963 vs. T6963C

NT7963	T6963C
Without dual mode: Without /DUAL, /ce1, /ce0 pins	**With dual mode**
Without 2-bit output data function: Without SDSEL, HOD pins	**With 2-bit output data function**

REVISION HISTORY

Version	Date	Revision	Page
Ver 0.1	7 Feb 2013	First release (Preliminary)	
Ver 0.2	10 Apr 2013	Add available PKG: NT7963KQ (LQFP-64L 7X7)	3, 34
Ver 1.0	17 Jul 2013	Built in feedback resister 1MΩ Add ordering information	2 3