40-Channel Segment / Common Driver For Dot Matrix LCD

Introduction

The NT7065B is a LCD driver IC which is fabricated by low power CMOS technology. Basically this IC consists of 20 x 2 bit bi-directional shift register, 20 x 2 bit data latch and 20 x 2 bit driver. This IC can be used as common or segment driver.

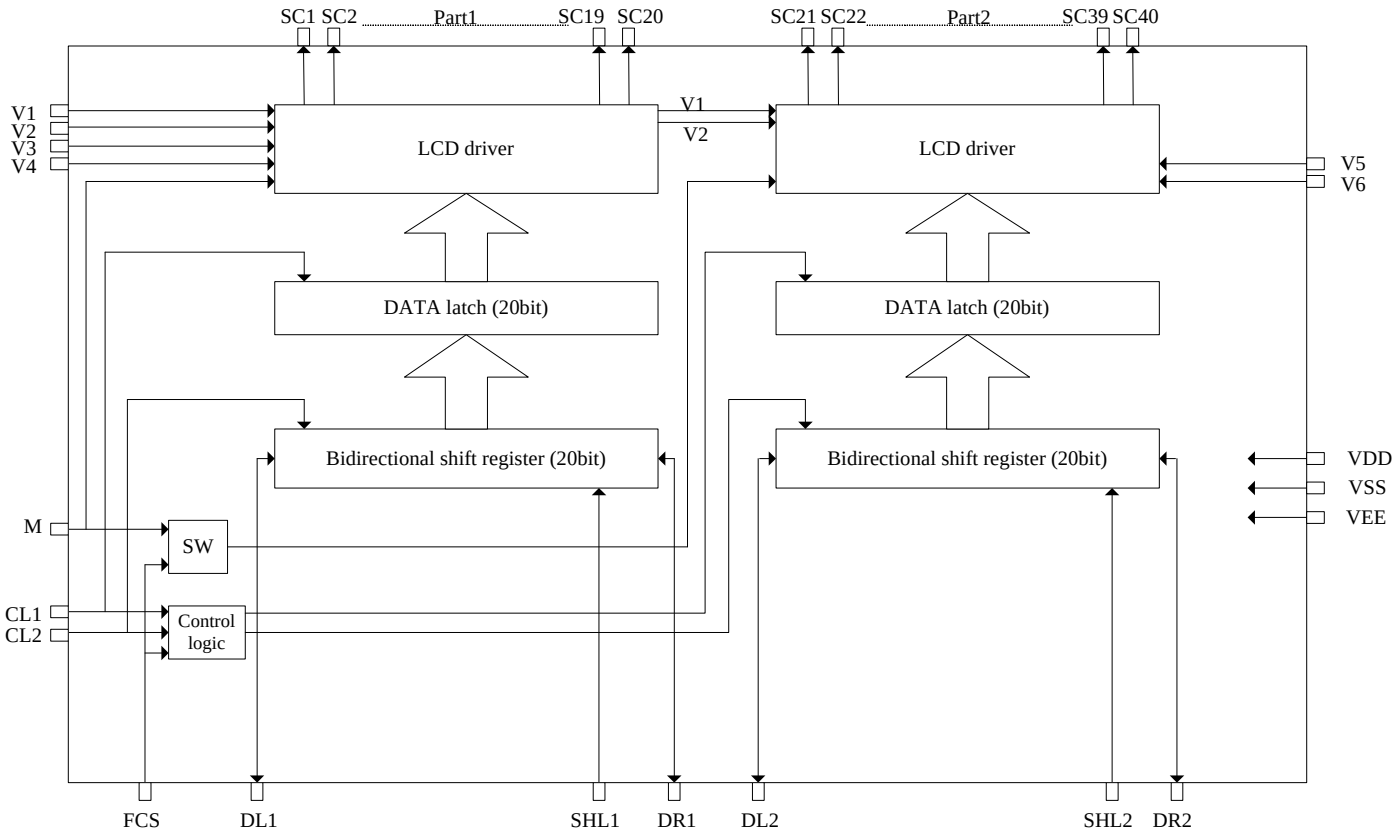
Function

- Dot matrix LCD driver with 40 channel output.
- Selects function to use common/segment drivers simultaneously.
- Input / Output signal.
  - -Output: 20 x 2 channel waveform for LCD driving
  - -Input: Serial display date and control signal from the controller LSI.
    Bias voltage (V1-V6)

Features

- Display driving bias: static~1/5
- Power supply voltage: 2.7~5.5V
- Supply voltage for display: 3~10V ($V_{LCD}=V_{DD}-V_{EE}$)
- Interface: (Controller NT7066U, NT7070B)
- CMOS Process
- Bare chip, 64QFP, and 64LQFP available

Block Diagram



Pin Description

<table>
<tr><th>PIN</th><th>INPUT/ OUTPUT</th><th colspan="2">NAME</th><th>DESCRIPTION</th><th>INTERFACE</th></tr>
<tr><td>V_{DD}</td><td rowspan="3">Power</td><td colspan="2" rowspan="2">Operating Voltage</td><td>For logical circuit (2.7~5.5V)</td><td rowspan="3">Power Supply</td></tr>
<tr><td>GND</td><td>0V(GND)</td></tr>
<tr><td>V_{EE}</td><td colspan="2">Negative Supply Voltage</td><td>For LCD driver circuit</td></tr>
<tr><td>V1,V2</td><td>Input</td><td colspan="2">Bias Voltage</td><td>Bias voltage level for LCD driver (select level)</td><td>Power</td></tr>
<tr><td>SC1~SC20</td><td>Output</td><td rowspan="3">Part1</td><td>LCD Driver</td><td>LCD driver output</td><td>LCD</td></tr>
<tr><td>V3,V4</td><td>Input</td><td>Bias Voltage</td><td>Bias voltage level for LCD drive (non-select level)</td><td>Power</td></tr>
<tr><td>SHL1</td><td>Input</td><td>Data Interface</td><td>Selection of the shift direction of part1 shift register
<table><tr><th>SHL1</th><th>DL1</th><th>DR1</th></tr><tr><td>V_{DD}</td><td>out</td><td>in</td></tr><tr><td>GND</td><td>in</td><td>out</td></tr></table></td><td>V_{DD} or GND</td></tr>
<tr><td>DL1,DR1</td><td>Input/ Output</td><td>Data input/output of part1 shift register</td><td>Controller or NT7065B</td></tr>
<tr><td>SC21~SC40</td><td>Output</td><td rowspan="3">Part2</td><td>LCD Driver</td><td>LCD driver output</td><td>LCD</td></tr>
<tr><td>V5,V6</td><td>Input</td><td>Bias Voltage</td><td>Bias voltage level for LCD drive (non-select level)</td><td>Power</td></tr>
<tr><td>SHL2</td><td>Input</td><td>Data Interface</td><td>Selection of the shift direction of part2 shift register
<table><tr><th>SHL2</th><th>DL2</th><th>DR2</th></tr><tr><td>V_{DD}</td><td>out</td><td>in</td></tr><tr><td>GND</td><td>in</td><td>out</td></tr></table></td><td>V_{DD} or GND</td></tr>
<tr><td>DL2,DL2</td><td>Input/ Output</td><td>Data input/output of part2 shift register</td><td>Controller or NT7065B</td></tr>
<tr><td>M</td><td>Input</td><td colspan="2">Alternated signal for LCD drive output</td><td rowspan="3"><table><tr><th>PART</th><th>FCS</th><th>CL1</th><th>CL2</th><th>M polarity</th></tr><tr><td rowspan="2">1</td><td>GND</td><td rowspan="2">Latch clock</td><td rowspan="2">Shift clock</td><td rowspan="2">M</td></tr><tr><td>V_{DD}</td></tr><tr><td rowspan="2">2</td><td>GND</td><td rowspan="2">Shift clock</td><td rowspan="2">Latch clock</td><td rowspan="2">—M</td></tr><tr><td>V_{DD}</td></tr></table>Shift/latch clock of display data and polarity of M signal are changed by FCS signal.
By setting FCS to V_{DD} level, user can select the function that use part1 as segment driver and part2 as common driver simultaneously.</td><td rowspan="3">Controller</td></tr>
<tr><td>CL1,CL2</td><td>Input</td><td colspan="2">Data shift/latch clock</td></tr>
<tr><td>FCS</td><td>Input</td><td colspan="2">Mode selection</td></tr>
</table>

Maximum Absolute Limit (Ta=25℃)

Characteristic	Symbol	Value	Unit
Power supply voltage	V_{DD}	-0.3~+7.0	V
Driver supply voltage	V_{EE}	V_{DD}-10.5~V_{DD}+0.3	V
Input voltage 1	V_{IN1}	-0.3~V_{DD}+0.3	V
Input voltage 2 (V1~V6)	V_{IN2}	V_{DD}+0.3~V_{EE}-0.3	V
Operating temperature	Topr	-30~+85	℃
Storage temperature	Tstg	-55~+125	℃

・Voltage grater than above may damage to the circuit

・VEE connect a protection resistor (220Ω±5%)

Electrical Characteristics

DC characteristics (V_{DD}=2.7~5.5V, V_{DD}-V_{EE}=3~10V, Ta=+25℃)

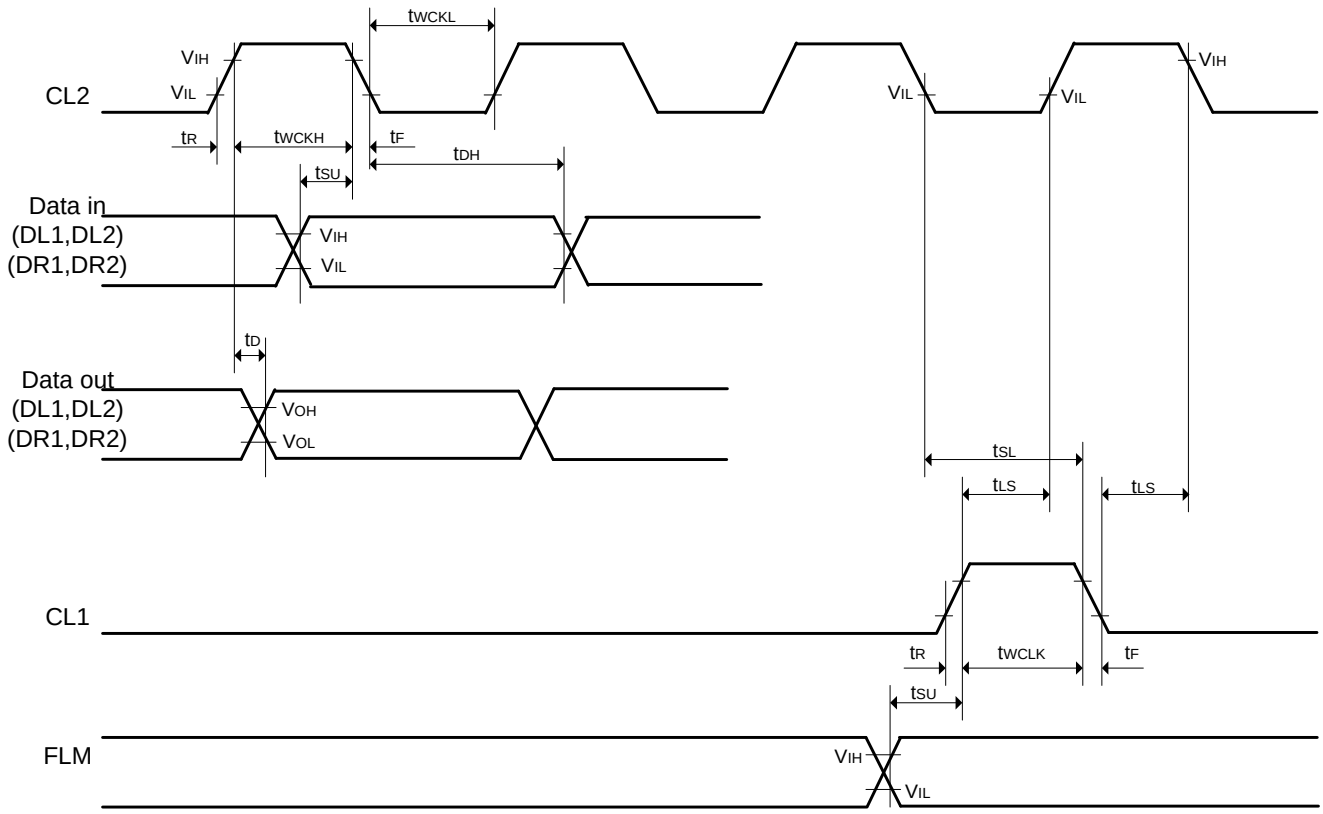
Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Operating current*	I_{DD}	f_{CL2}=400KHz	-	1	mA	-
Supply current*	I_{EE}	f_{CL1}=1KHz	-	10	μA	
Input high voltage	V_{IH}	-	0.7V_{DD}	V_{DD}	V	CL1,CL2,DL1, DL2,DR1,DR2, SHL1,SHL2,M, FCS
Input low voltage	V_{IL}		0	0.3V_{DD}		
Input leakage current	I_{LKG}	V_{IN}=0~VDD	-5	5	μA	
Output high voltage	V_{OH}	I_{OH}=-0.4mA	V_{DD}-0.4	-	V	DL1,DL2,DR1, DR2
Output low voltage	V_{OL}	I_{OL}=+0.4mA	-	0.4		
Voltage descending	V_{D1}	I_{ON}=0.1mA for one of SC1~SC40	-	1.1		V(V1~V6)-SC(SC1~SC40)
	V_{D2}	I_{ON}=0.05mA for each SC1~SC40	-	1.5		
Leakage current	I_V	V_{IN}=V_{DD}~V_{EE} (output SC1~SC40 : floating)	-10	10	μA	V1~V6

*Input/Output current is excluded; When input at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply, To avoid this, input level must be fixed at “H” or “L”.

AC characteristics (V_{DD}=2.7~5.5V, V_{DD}-V_{EE}=3~10V, Ta=+25℃)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Data shift frequency	f_{CL}	-	-	400	KHz	CL2
Clock high level width	t_{WCKH}	-	800	-	nS	CL1, CL2
Clock low level width	t_{WCKL}	-	800	-		CL2
Clock set-up time	t_{SL}	From CL2 to CL1	500	-		CL1, CL2
	t_{LS}	From CL1 to CL2	500	-		
Clock rise/fall time	t_R/t_F	-	-	200		
Data set-up time	t_{SU}	-	300	-		DL1,DL2,DR1, DR2,FLM
Data hold time	t_{DH}	-	300	-		
Data delay time	t_D	CL=15pF	-	500		DL1,DL2,DR1, DR2

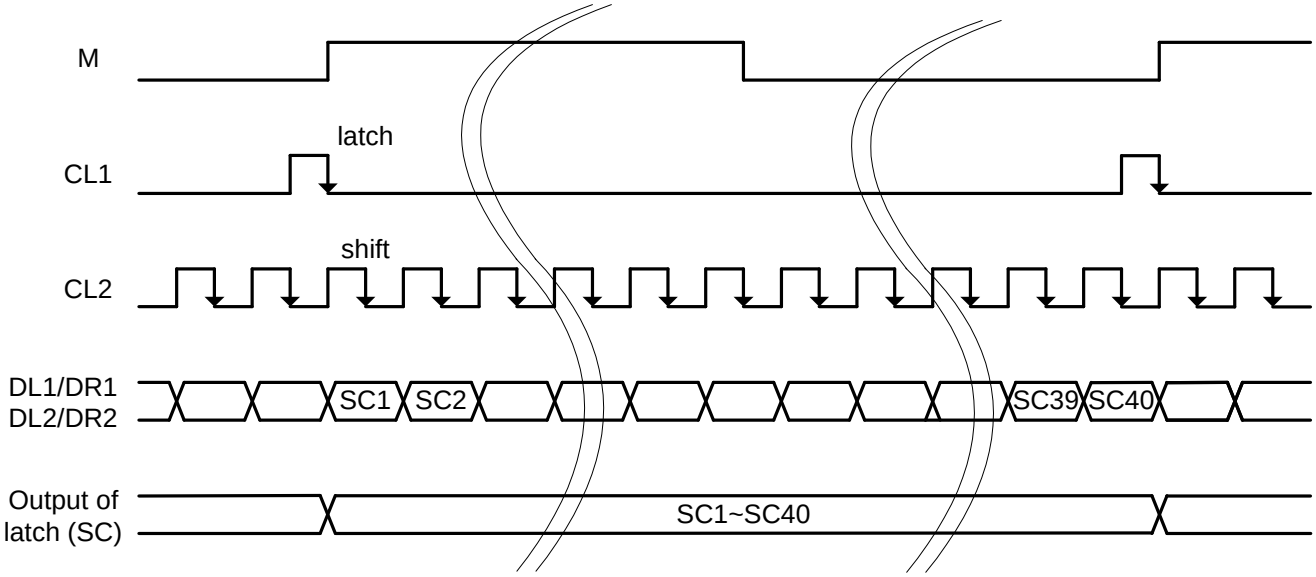
Timing Characteristics



Functional Description

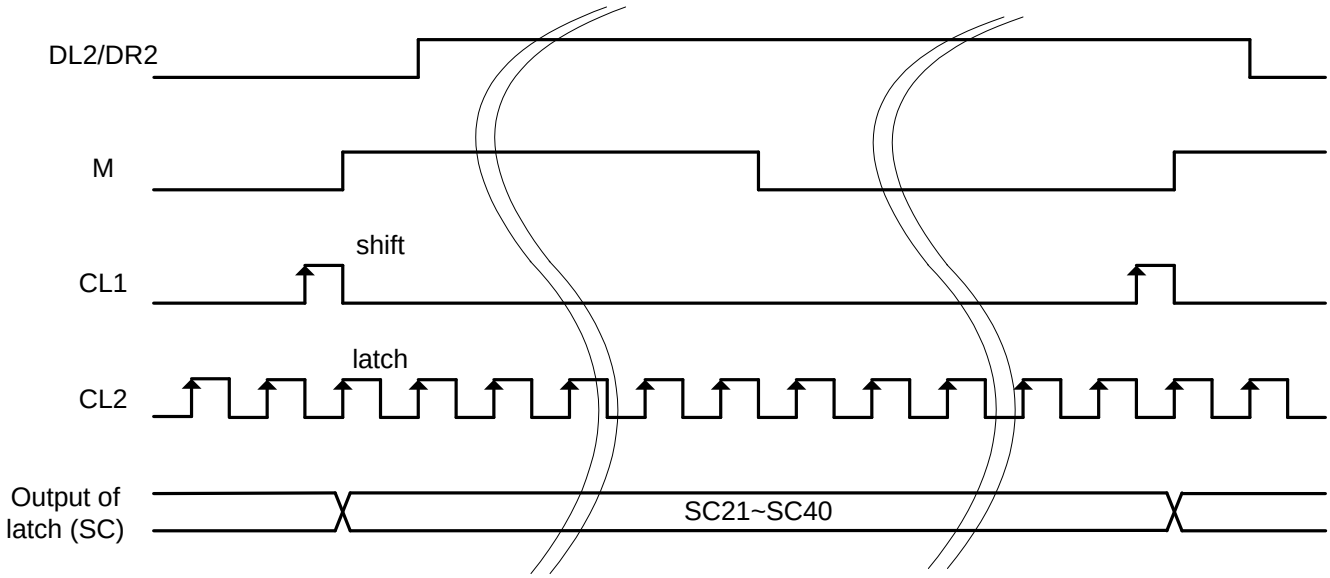
1) To drive segment type

When the FCS is connected to GND, NT7065B (SC1~SC40) is operated as segment driver.

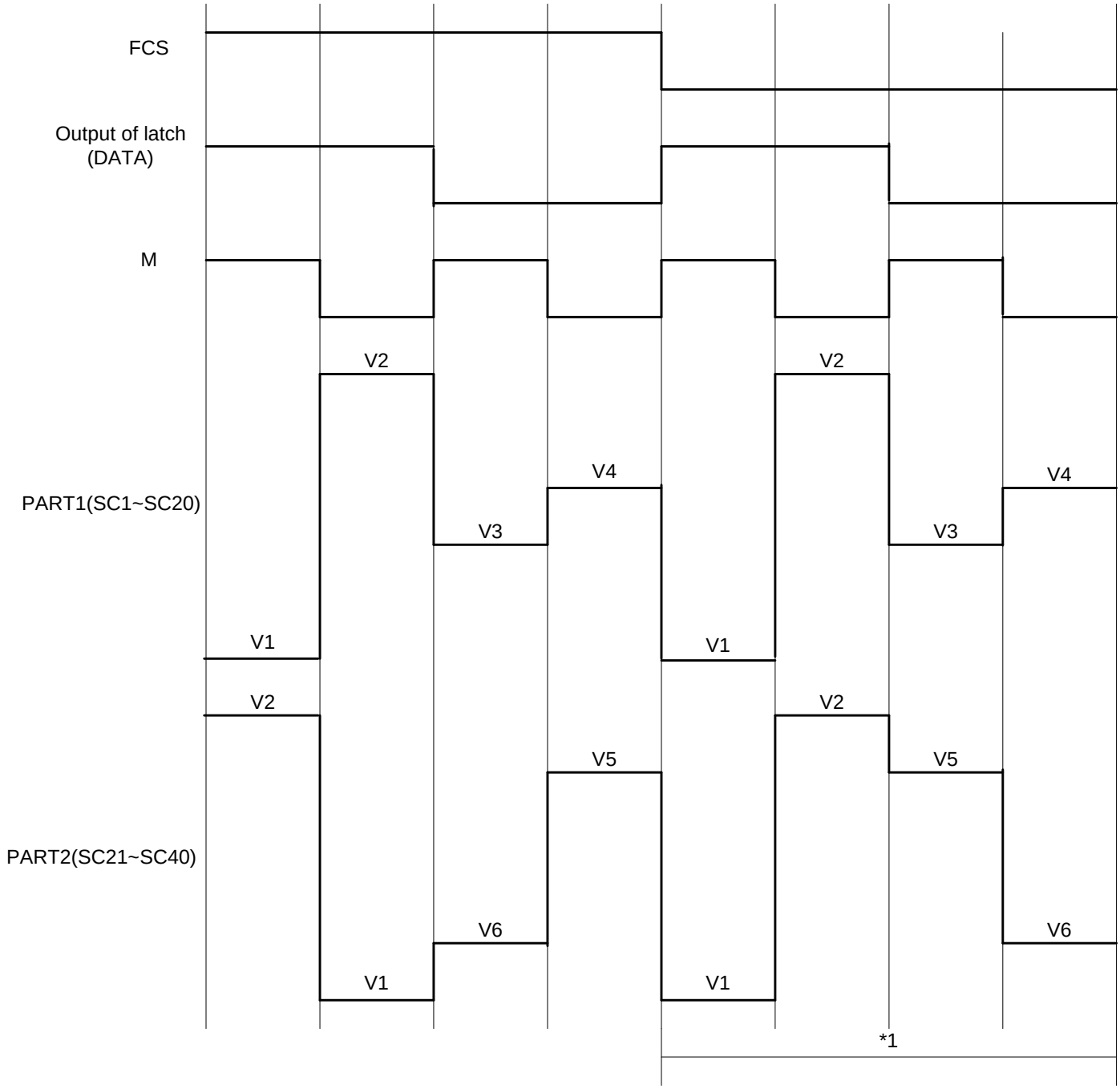


2) To drive common type

When the FCS is connected to V_{DD}, only part2 (SC21~SC40) of NT7065B is operated as common driver.



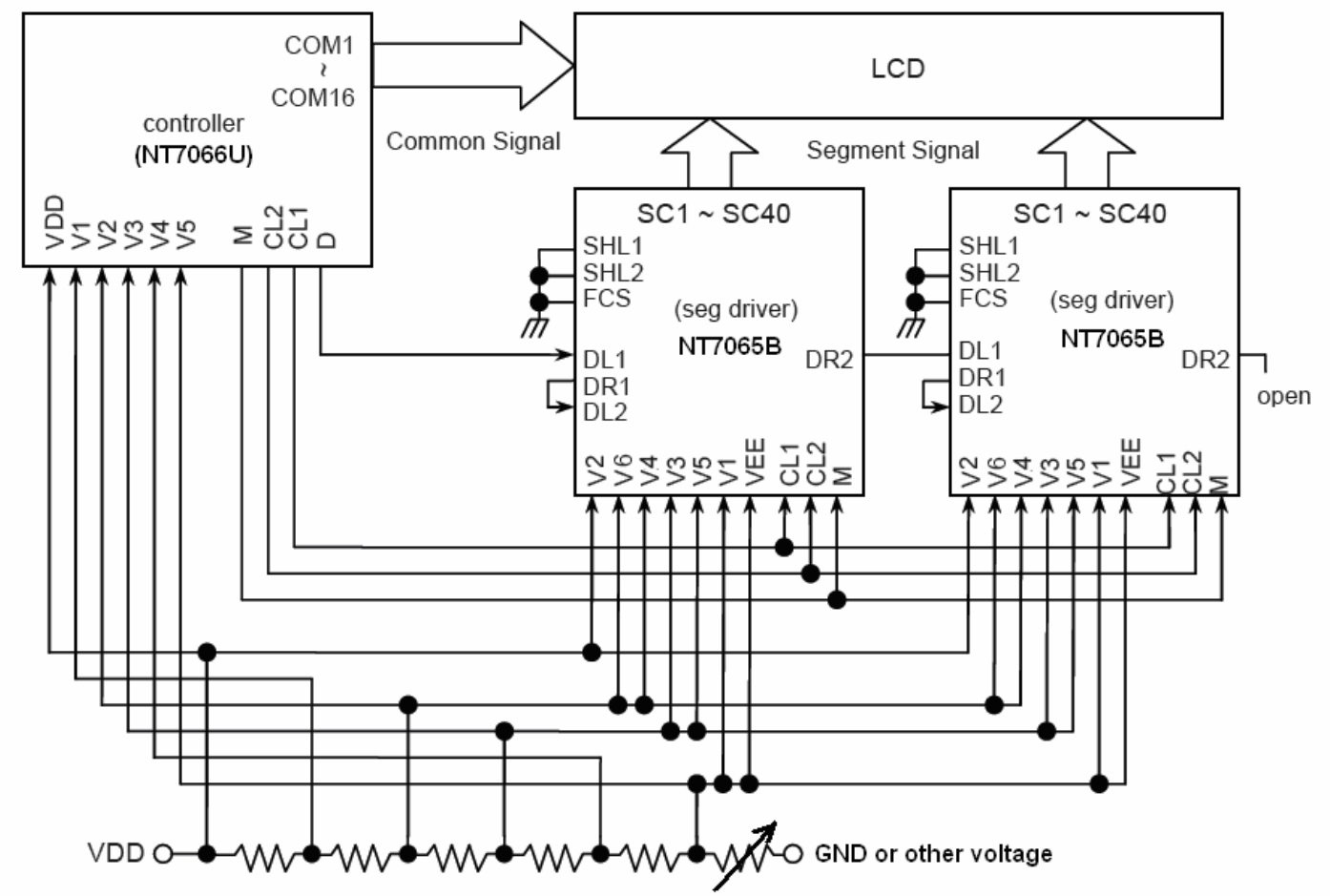
LCD Output Waveforms



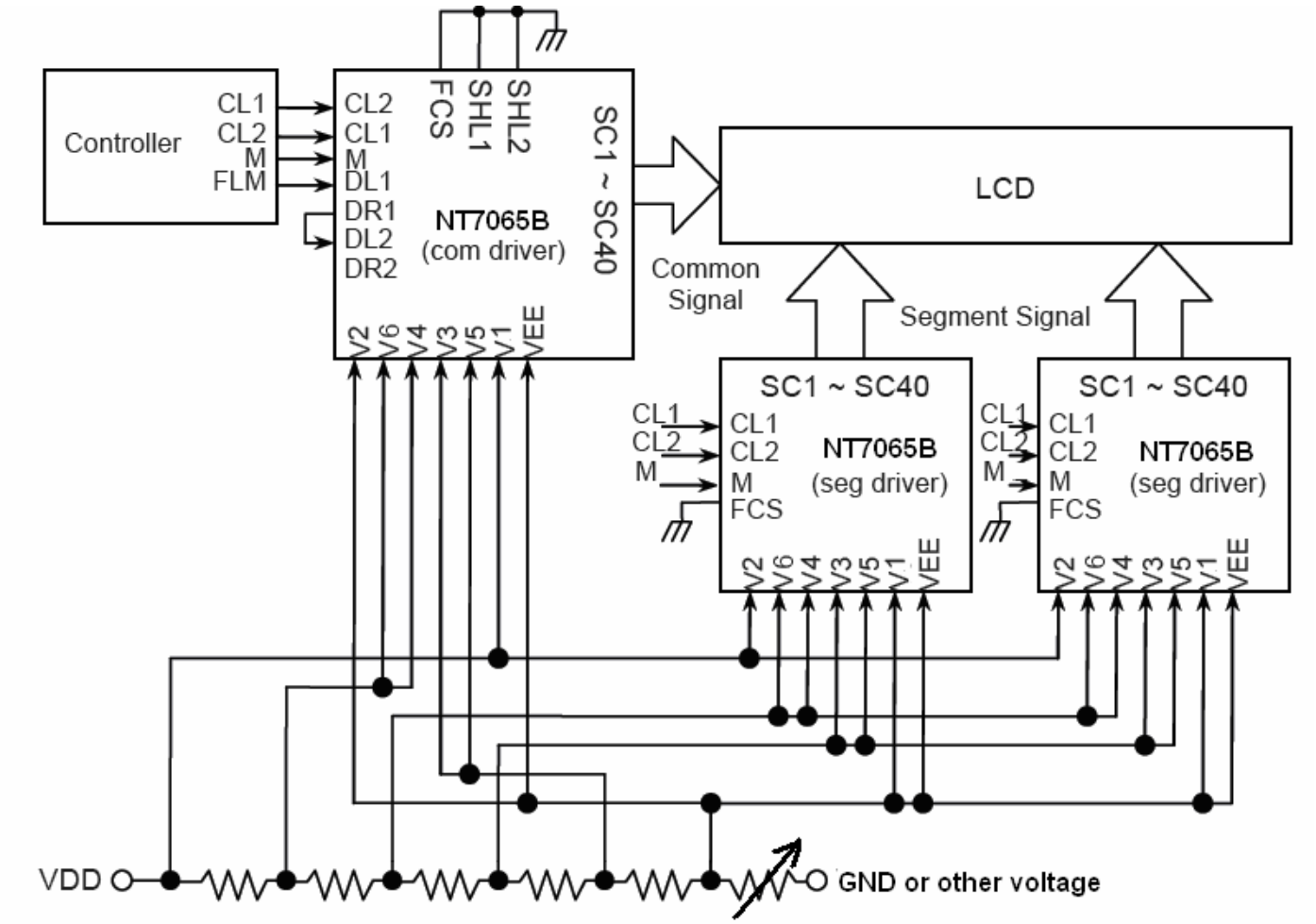
*1: To use for same function of part1 and part2, V3 and V5, V4 and V6 of power supply for LCD driver are short circuited respectively.

Application circuit

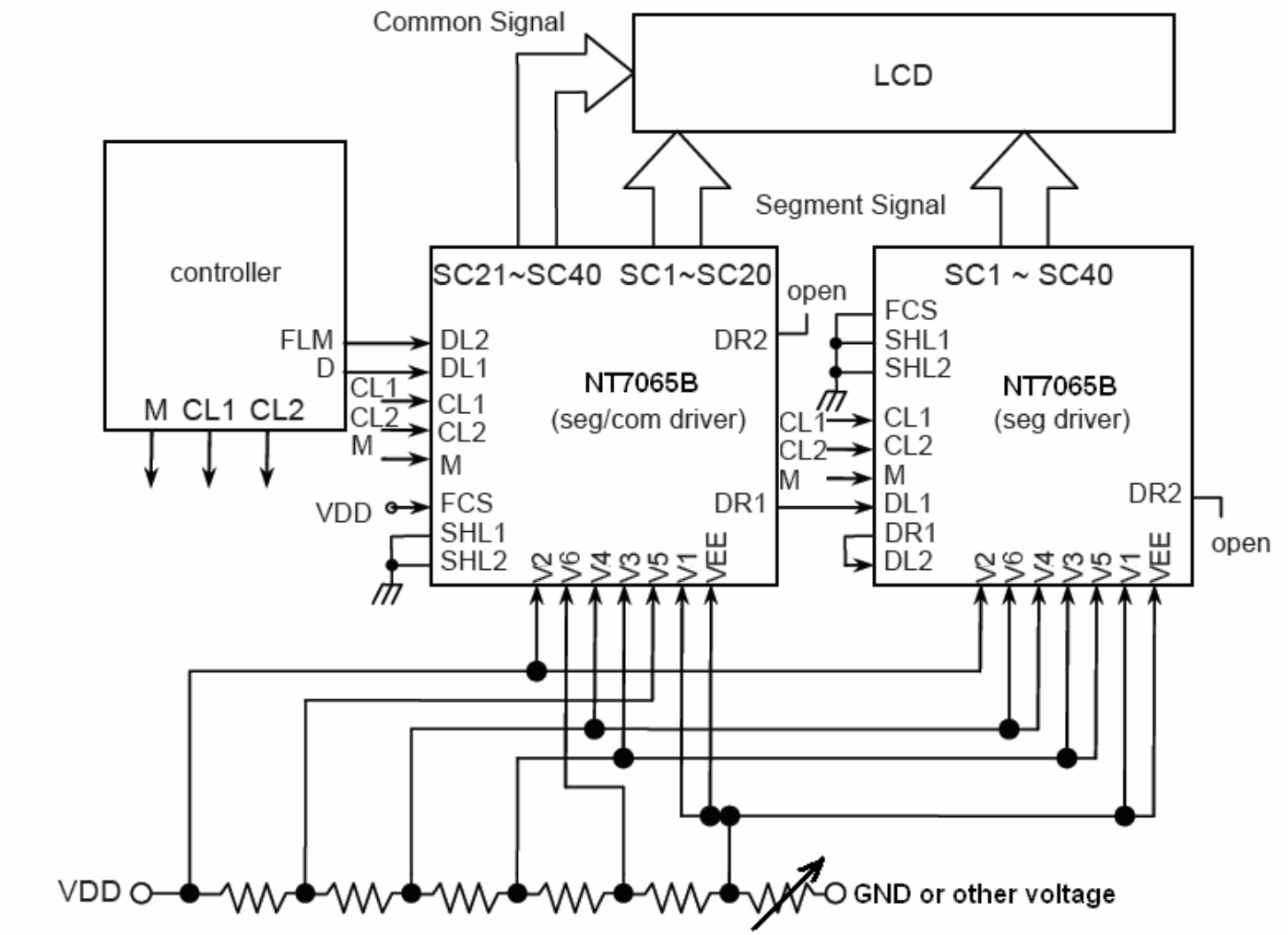
1) Segment driver



2) Common driver

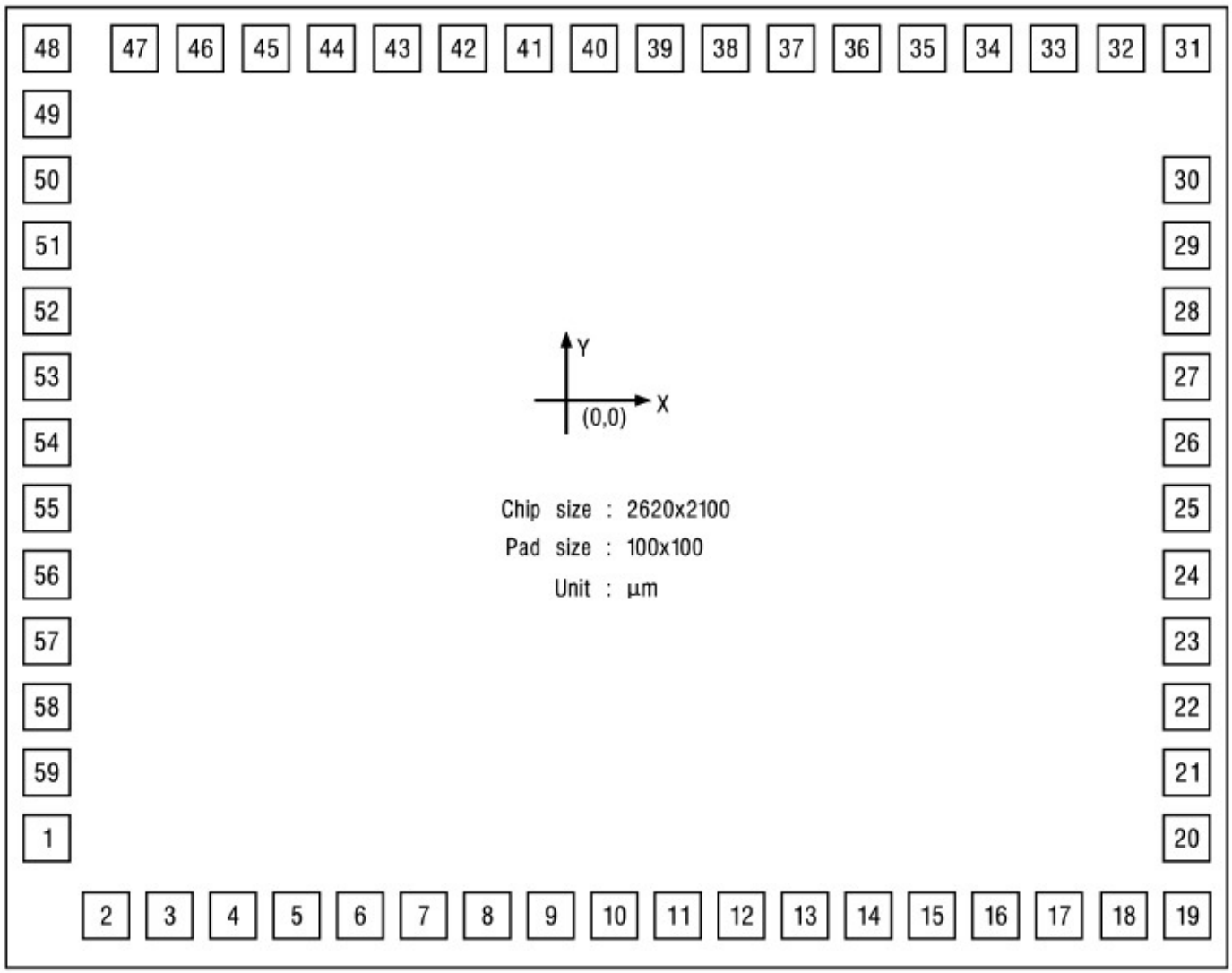


3) Segment/Common driver



Pad Diagram

Note: Please connects the substrate to V_{DD} or floating

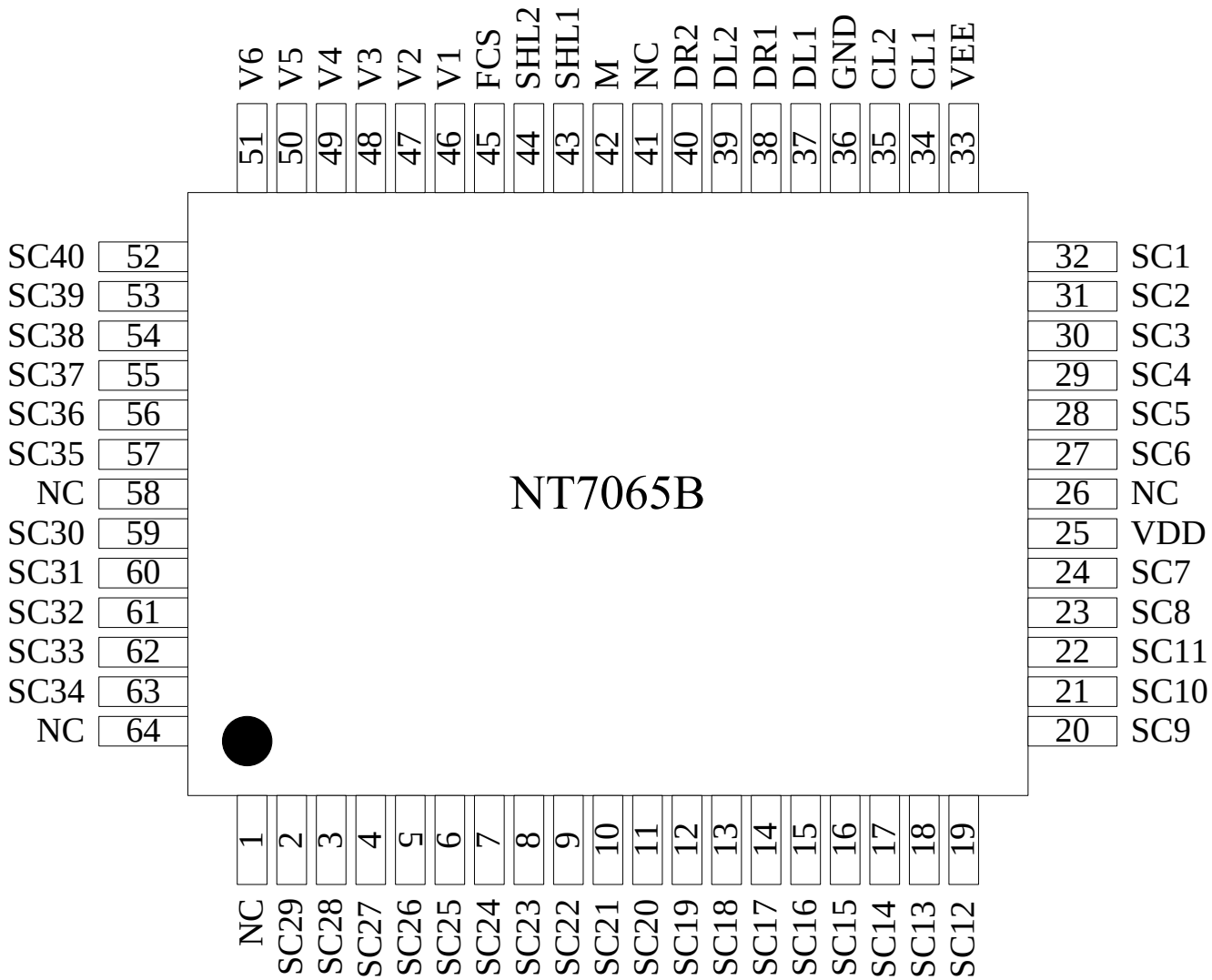


Pad Location

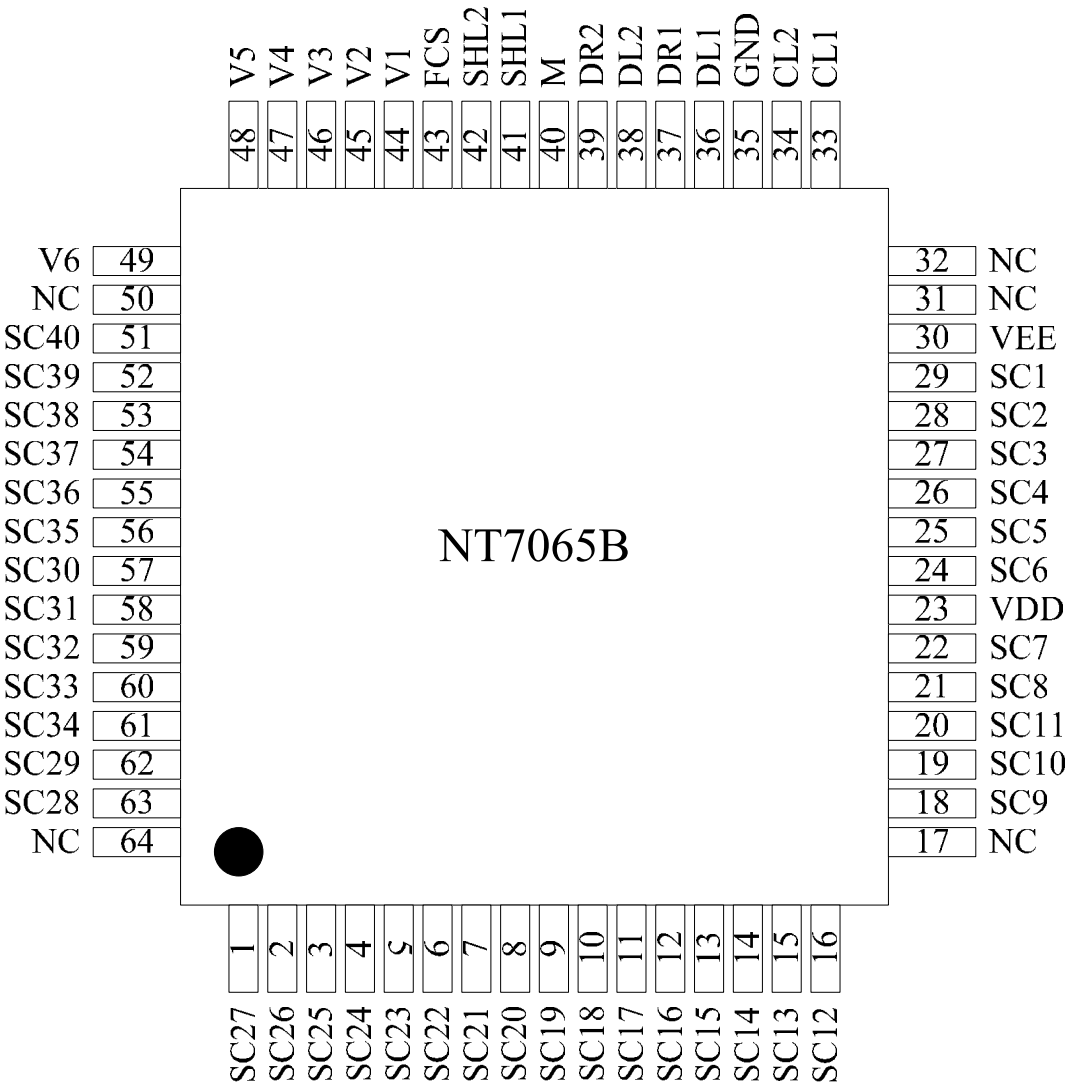
Note: (0,0) is center in the chip

Pad		Coordinates		Pad		Coordinates	
NO.	Name	X	Y	NO.	Name	X	Y
1	VEE	-1120.20	-642.50	31	SC28	1117.50	865.20
2	CL1	-1062.50	-865.20	32	SC27	992.50	865.20
3	CL2	-937.50	-865.20	33	SC26	867.50	865.20
4	GND	-812.50	-865.20	34	SC25	742.50	865.20
5	DL1	-687.50	-865.20	35	SC24	617.50	865.20
6	DR1	-562.50	-865.20	36	SC23	492.50	865.20
7	DL2	-437.50	-865.20	37	SC22	367.50	865.20
8	DR2	-312.50	-865.20	38	SC21	242.50	865.20
9	M	-187.50	-865.20	39	SC20	117.50	865.20
10	SHL1	-62.50	-865.20	40	SC19	-7.50	865.20
11	SHL2	62.50	-865.20	41	SC18	-132.50	865.20
12	FCS	187.50	-865.20	42	SC17	-257.50	865.20
13	V1	332.50	-865.20	43	SC16	-382.50	865.20
14	V2	457.50	-865.20	44	SC15	-507.50	865.20
15	V3	582.50	-865.20	45	SC14	-632.50	865.20
16	V4	707.50	-865.20	46	SC13	-757.50	865.20
17	V5	832.50	-865.20	47	SC12	-882.50	865.20
18	V6	957.50	-865.20	48	SC9	-1120.20	857.20
19	SC40	1082.50	-865.20	49	SC10	-1120.20	732.50
20	SC39	1120.20	-627.50	50	SC11	-1120.20	607.50
21	SC38	1120.20	-502.50	51	SC8	-1120.20	482.50
22	SC37	1120.20	-377.50	52	SC7	-1120.20	357.50
23	SC36	1120.20	-252.50	53	VDD	-1120.20	232.50
24	SC35	1120.20	-127.50	54	SC6	-1120.20	107.50
25	SC30	1120.20	-2.50	55	SC5	-1120.20	-17.50
26	SC31	1120.20	122.50	56	SC4	-1120.20	-142.50
27	SC32	1120.20	247.50	57	SC3	-1120.20	-267.50
28	SC33	1120.20	372.50	58	SC2	-1120.20	-392.50
29	SC34	1120.20	479.50	59	SC1	-1120.20	-517.50
30	SC29	1120.20	622.50				

Pin Configuration (64QFP)



Pin Configuration (64LQFP)

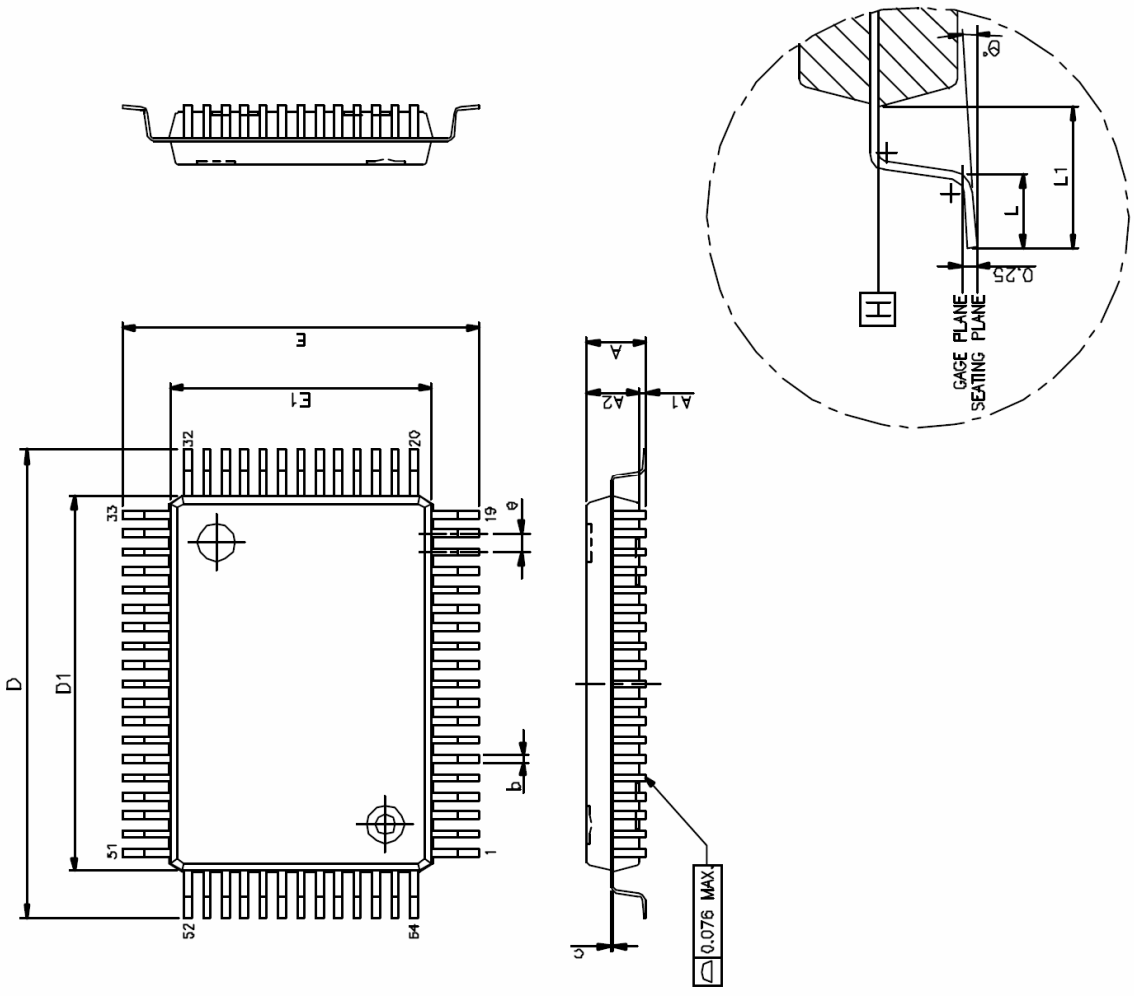


64QFP Outline Dimension

SYMBOLS	MIN.	NOM	MAX.
A	–	–	3.40
A1	0.25	–	–
A2	2.55	2.72	3.05
b	0.35	0.40	0.50
c	0.11	0.15	0.23
D		25.00 BASIC	
D1		20.00 BASIC	
e		1.00 BASIC	
E		19.00 BASIC	
E1		14.00 BASIC	
L	1.15	1.30	1.45
L1		2.50 REF	
θ°	0	3.5	7

UNIT : mm

NOTES:
1.JEDEC : N/A.
2.DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H .
4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION .



64LQFP Outline Dimension

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)			
SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D		9.00 BSC	
D1		7.00 BSC	
e		0.40 BSC	
E		9.00 BSC	
E1		7.00 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

NOTES:
1.JEDEC OUTLINE : MS-026 BBD
2.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.