Introduction

The NT7063B is a LCD driver LSI which is fabricated by low power CMOS technology. Basically this LSI consists of 40 x 2 bit bidirectional shift register, 40 x 2 bit data latch and 40 x 2 bit LCD driver (refer to Fig 1). This LSI can be used segment driver.

Function

- Dot matrix LCD driver with 80 channel output.
- Input/Output signal

  Output: 40 x 2 channel waveform for LCD driving

  Input: Serial display data and control pulse from the controller LSI.

  Bias voltage (V_1 - V_4)

Features

- Display driving bias: static ~1/5
- Power supply voltage: 2.7V~5.5V
- Supply voltage for display: V_{DD} ~ -5V (V_{EE})
- Interface

driver (cascade connection)	controller
NT7065B, Other NT7063B	NT7066U

- CMOS Process
- Bare chip, 100QFP, 100LQFP

Block Diagram

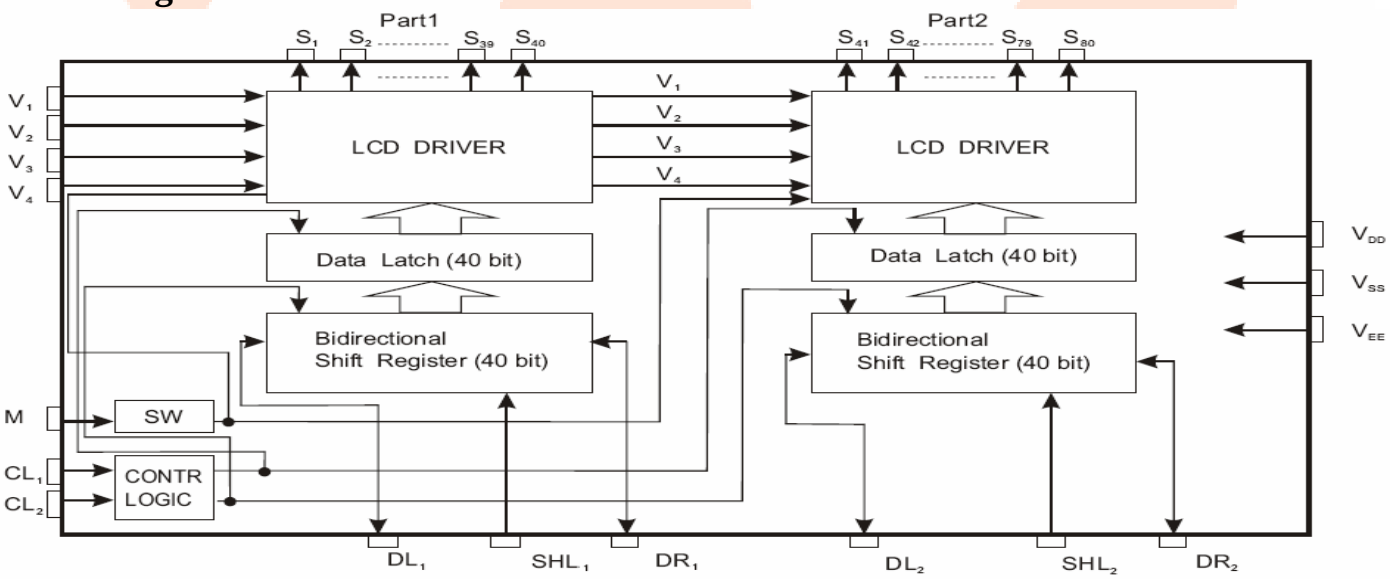


Fig 1. NT7063B functional block diagram

Pin Description

Symbol	Input Output	Name		Description	Interface
V_{DD}	Power	Operating Voltage		For logical circuit (2.7V~5.5V)	Power supply
V_{SS} (GND)				0V (GND)	
V_{EE}		Negative Supply Voltage		For LCD driver circuit (V_{DD} ~ -5V)	
V1, V2	Input	LCD driver output voltage level		Bias voltage level for LCD driver (select level)	Power
V3, V4	Input			Bias voltage level for LCD driver (nonselect level)	
S1~S40	Output	Part1	LCD driver	LCD driver output	LCD
SHL1	Input		Data interface	Selection of the shift direction of shift register	V_{DD} or V_{SS}
DL1, DR1	Input Output			Data input/output of shift register (part1)	Controller or NT7063B/65B
S41~S80	Output	Part2	LCD driver	LCD driver output	LCD
SHL2	Input		Data interface	Selection of the shift direction of shift register	V_{DD} or V_{SS}
DL2, DR2	Input Output			Data input/output of shift register (part2)	Controller or NT7063B/65B
M	Input	Alternated signal for LCD driver Output		The alternating signal to convert LCD drive waveform to AC	Controller
CL1, CL2	Input	Data shift/latch clock		CL1: Data latch clock CL2: Data shift clock	

Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit
Operating voltage	V_{DD}	-0.3~+7.0	V
Driver supply voltage	V_{EE}	-6.0~V_{DD}+0.3	
Input voltage 1	V_{IN1}	-0.3~V_{DD}+0.3	
Input voltage 2 (V1~V4)	V_{IN2}	V_{DD}+0.3~V_{EE}-0.3	
Operating temperature	T_{OPR}	-30~+85	℃
Storage temperature	T_{STG}	-55~+125	

***Voltage grater than above may damage to the circuit.**

***V_{EE}: connect a protection resister (220Ω±5%)**

Electrical Characteristics

DC Characteristics (V_{DD}=2.7V~5.5V, V_{EE}=-5V, V_{SS}=0V, Ta=-30~85℃)

Characteristic	Symbol	Test Condition	Min.	Max.	Unit	Applicable pin
Operating Current	I_{DD}	f_{CL2}=400KHz	-	1	mA	V_{DD},V_{EE}
Supply Current	I_{EE}	f_{CL1}=1KHz	-	10	uA	
Input High Voltage	V_{IH}		0.7V_{DD}	V_{DD}	V	CL1,CL2,DL1, DL2,DR1,DR2, SHL1,SHL2,M
Input Low Voltage	V_{IL}		0	0.3V_{DD}		
Input Leakage Current	I_{LKG}	V_{IN}=0~VDD	-5	5	uA	
Output High Voltage	V_{OH}	I_{OH}=-0.4mA	V_{DD}-0.4	-	V	DL1,DL2, DR1,DR2,
Output Low Voltage	V_{OL}	I_{OL}=+0.4mA	-	0.4		
Voltage Descending	V_{D1}	I_{ON}=0.1mA for one of S1~S80		1.1		S1~S80
	V_{D2}	I_{ON}=0.05mA for one of S1~S80		1.5		
Leakage Current	I_V	V_{IN}=V_{DD}~V_{EE} (Output S1~S80; floating)	-10	10	uA	V1~V4

AC Characteristics (V_{DD}=2.7V~5.5V, V_{EE}=-5V, V_{SS}=0V, Ta=-30~85℃)

Characteristic	Symbol	Test Condition	Min.	Max.	Unit	Applicable pin
Data Shift Frequency	f_{CL}		-	400	KHz	CL2
Clock High Level Width	t_{WCKH}		800	-	ns	CL1,CL2
Clock Low level Width	t_{WCKL}		800	-		CL2
Clock Set-up Time	t_{SL}	From CL2 to CL1	500	-		CL1,CL2
	t_{LS}	From CL1 to CL2	500	-		
Clock Rise/Fall Time	t_R/t_F		-	200		
Data Set-up Time	t_{SU}		300	-		DL1,DL2, DR1,DR2
Data Hold Time	t_{DH}		300	-		
Data Delay Time	t_D	C_L=15pF	-	500		

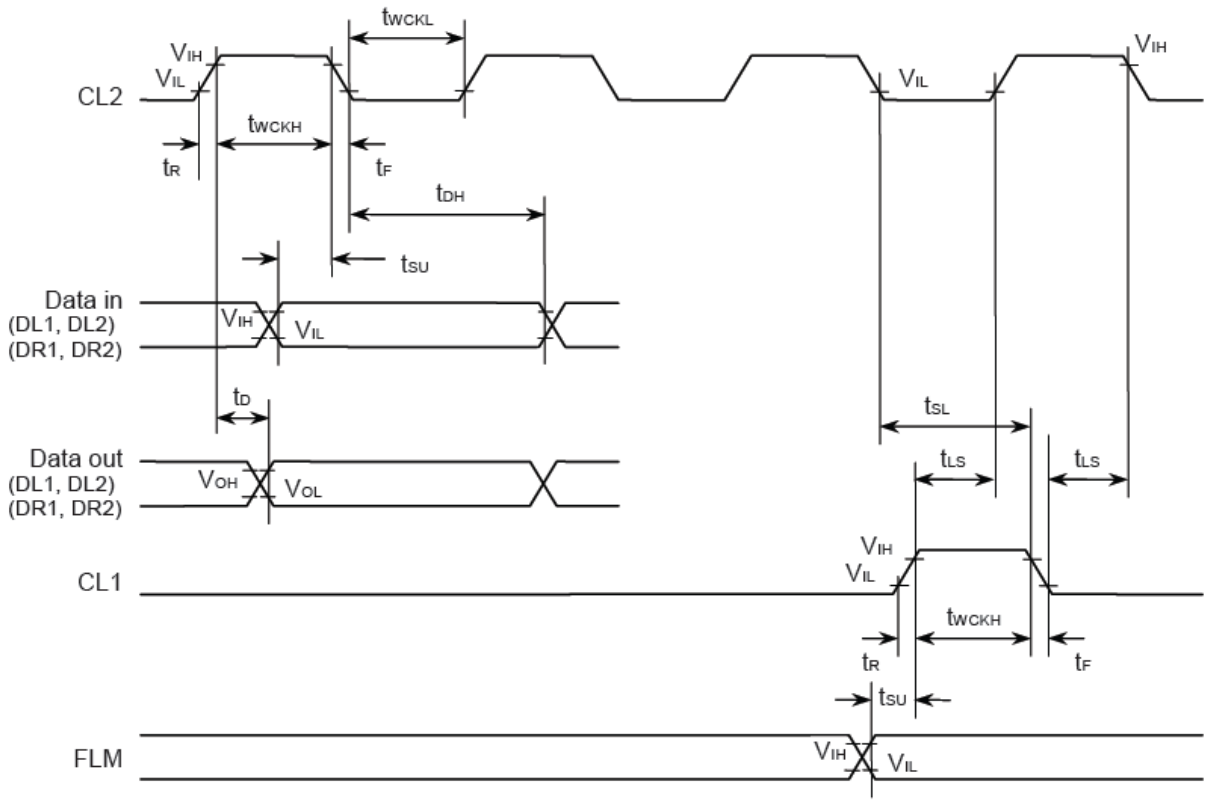
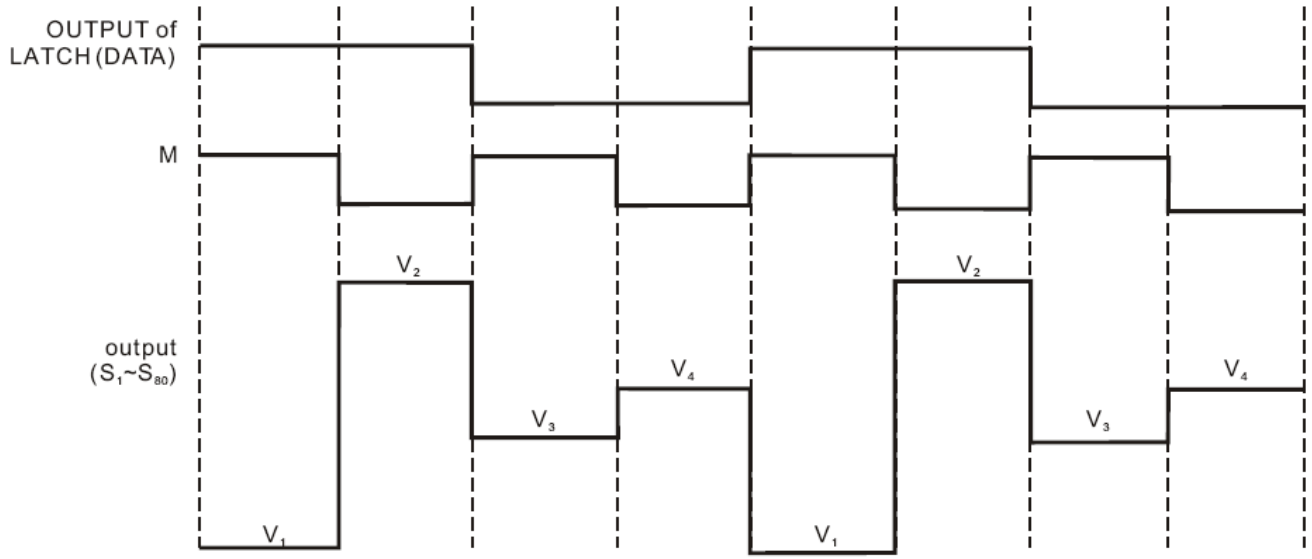
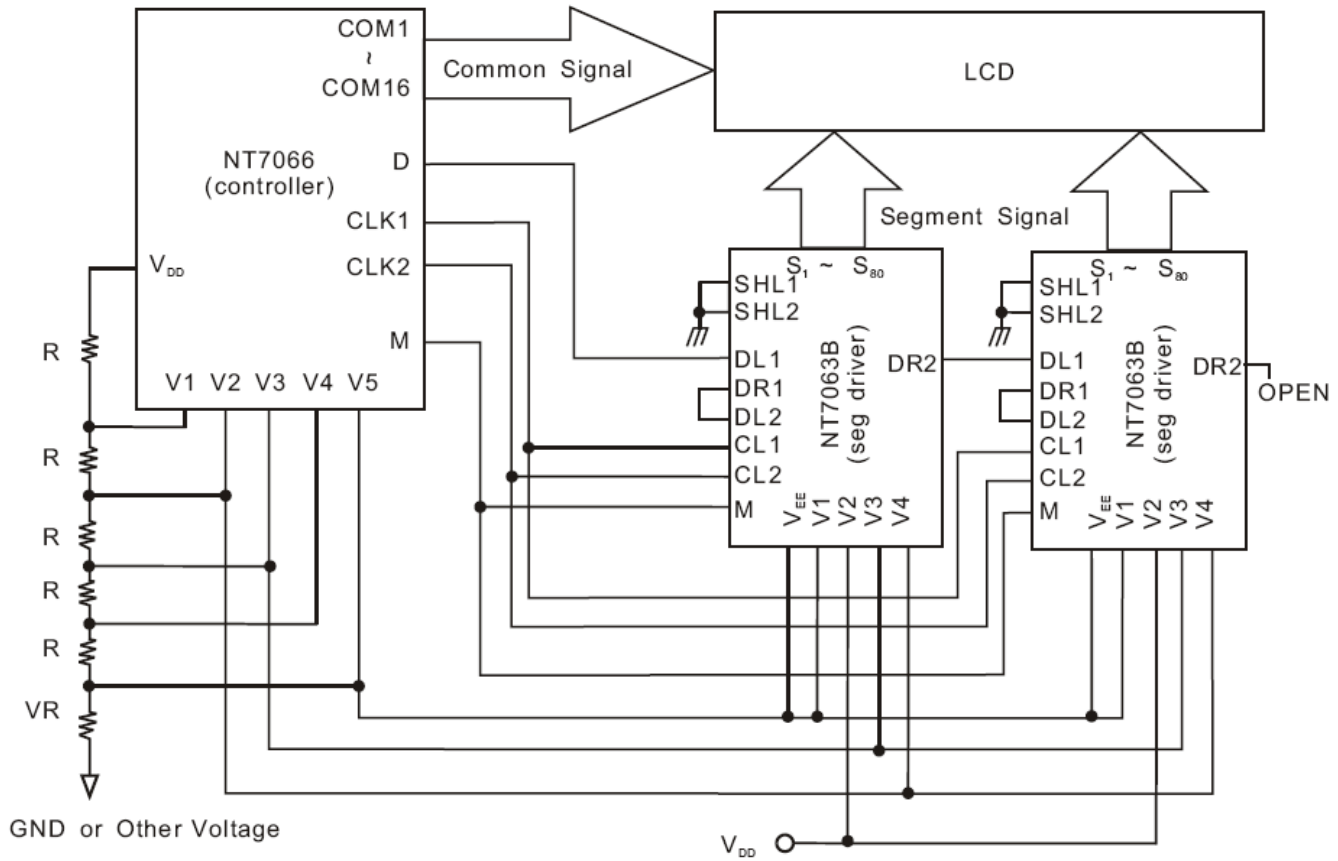


Fig 2. AC characteristics

LCD Output Waveforms

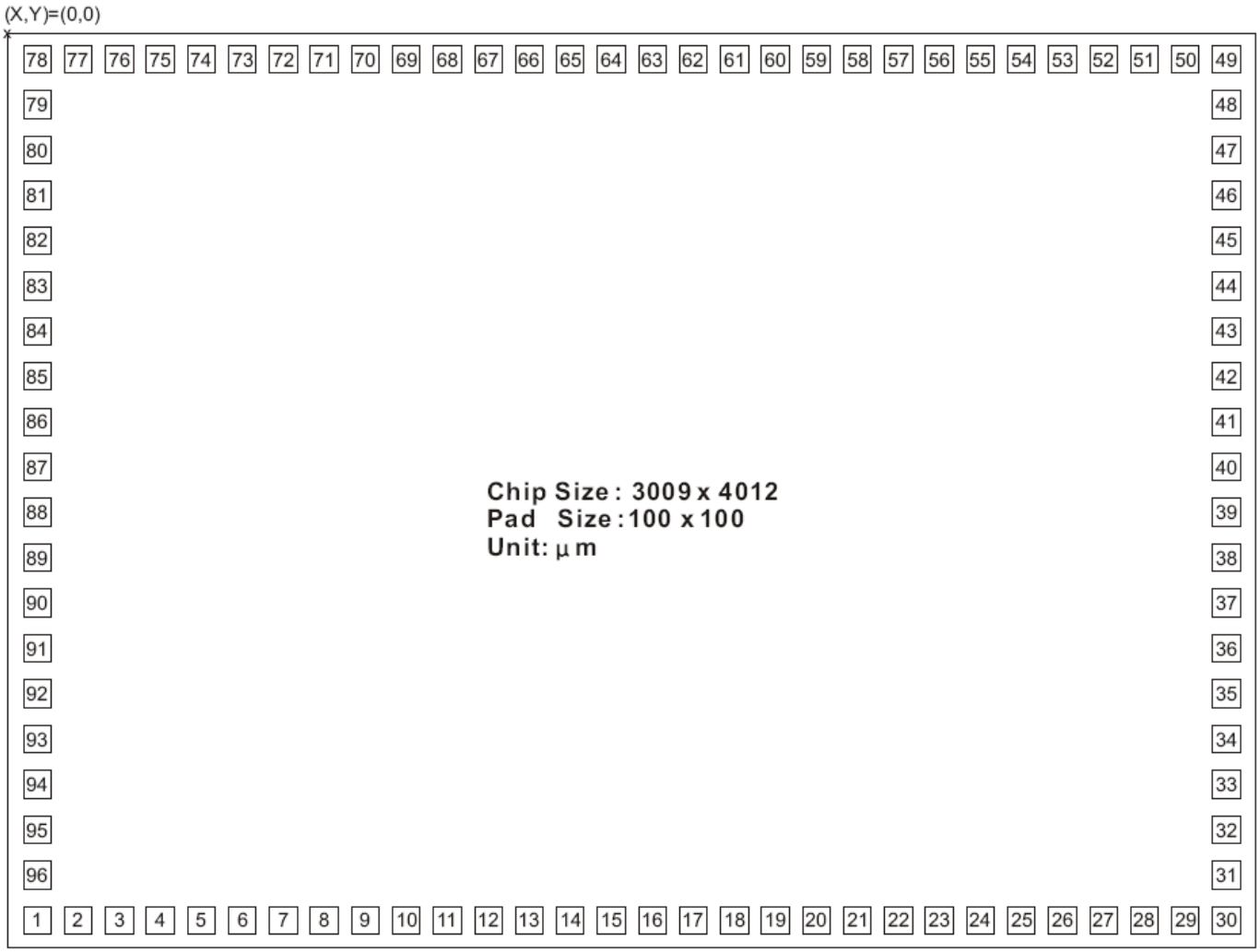


Application Circuit



Pad Diagram

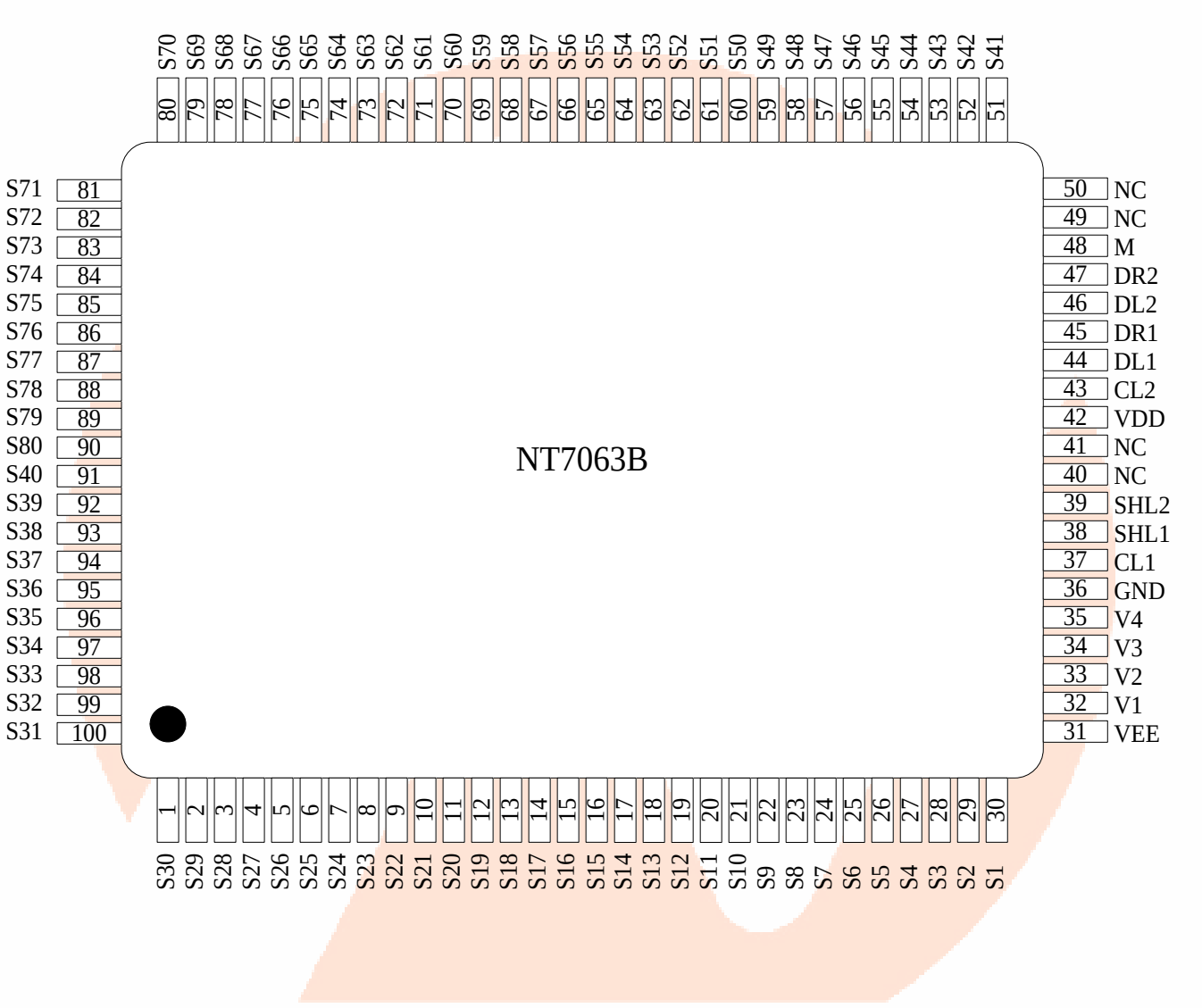
Note: Please connects the substrate to V_{DD} or floating



Pad Location

Pad Number	Pad Name	X	Y	Pad Number	Pad Name	X	Y
1	S42	2860.00	157.25	49	S31	148.75	3854.75
2	S43	2860.00	284.75	50	S30	148.75	3727.25
3	S44	2860.00	412.25	51	S29	148.75	3599.75
4	S45	2860.00	539.75	52	S28	148.75	3472.25
5	S46	2860.00	667.25	53	S27	148.75	3344.75
6	S47	2860.00	794.75	54	S26	148.75	3217.25
7	S48	2860.00	922.25	55	S25	148.75	3089.75
8	S49	2860.00	1049.75	56	S24	148.75	2962.25
9	S50	2860.00	1177.25	57	S23	148.75	2834.75
10	S51	2860.00	1304.75	58	S22	148.75	2707.25
11	S52	2860.00	1432.25	59	S21	148.75	2579.75
12	S53	2860.00	1559.75	60	S20	148.75	2452.25
13	S54	2860.00	1587.25	61	S19	148.75	2324.75
14	S55	2860.00	1814.75	62	S18	148.75	2197.25
15	S56	2860.00	1942.25	63	S17	148.75	2069.75
16	S57	2860.00	2069.75	64	S16	148.75	1942.25
17	S58	2860.00	2197.25	65	S15	148.75	1814.75
18	S59	2860.00	2324.75	66	S14	148.75	1687.25
19	S60	2860.00	2452.25	67	S13	148.75	1559.75
20	S61	2860.00	2579.75	68	S12	148.75	1432.25
21	S62	2860.00	2707.25	69	S11	148.75	1304.75
22	S63	2860.00	2834.75	70	S10	148.75	1177.25
23	S64	2860.00	2962.25	71	S9	148.75	1049.75
24	S65	2860.00	3089.75	72	S8	148.75	922.25
25	S66	2860.00	3217.25	73	S7	148.75	794.75
26	S67	2860.00	3344.75	74	S6	148.75	667.25
27	S68	2860.00	3472.25	75	S5	148.75	539.75
28	S69	2860.00	3599.75	76	S4	148.75	412.25
29	S70	2860.00	3727.25	77	S3	148.75	284.75
30	S71	2860.00	3854.75	78	S2	148.75	157.25
31	S72	2588.25	3867.50	79	S1	403.75	144.50
32	S73	2460.75	3867.50	80	VEE	531.25	144.50
33	S74	2333.25	3867.50	81	V1	658.75	144.50
34	S75	2205.75	3867.50	82	V2	786.25	144.50
35	S76	2078.25	3867.50	83	V3	913.75	144.50
36	S77	1950.75	3867.50	84	V4	1041.25	144.50
37	S78	1823.25	3867.50	85	GND	1168.75	144.50
38	S79	1695.75	3867.50	86	CL1	1313.25	144.50
39	S80	1568.25	3867.50	87	SHL1	1440.75	144.50
40	S40	1440.75	3867.50	88	SHL2	1568.25	144.50
41	S39	1313.25	3867.50	89	VDD	1695.75	144.50
42	S38	1185.75	3867.50	90	CL2	1823.25	144.50
43	S37	1058.25	3867.50	91	DL1	1950.75	144.50
44	S36	930.75	3867.50	92	DR1	2078.25	144.50
45	S35	803.25	3867.50	93	DL2	2205.75	144.50
46	S34	675.75	3867.50	94	DR2	2333.25	144.50
47	S33	548.25	3867.50	95	M	2460.75	144.50
48	S32	420.75	3867.50	96	S41	2605.25	144.50

Pin Configuration (100 QFP)

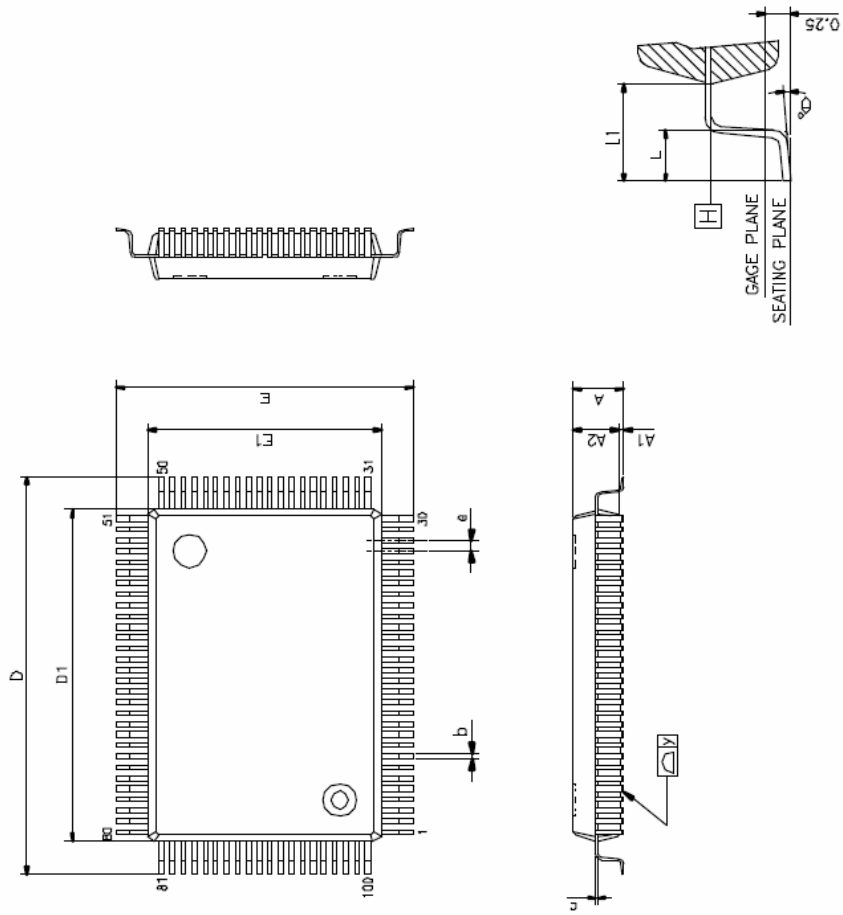


100 QFP Outline Dimension

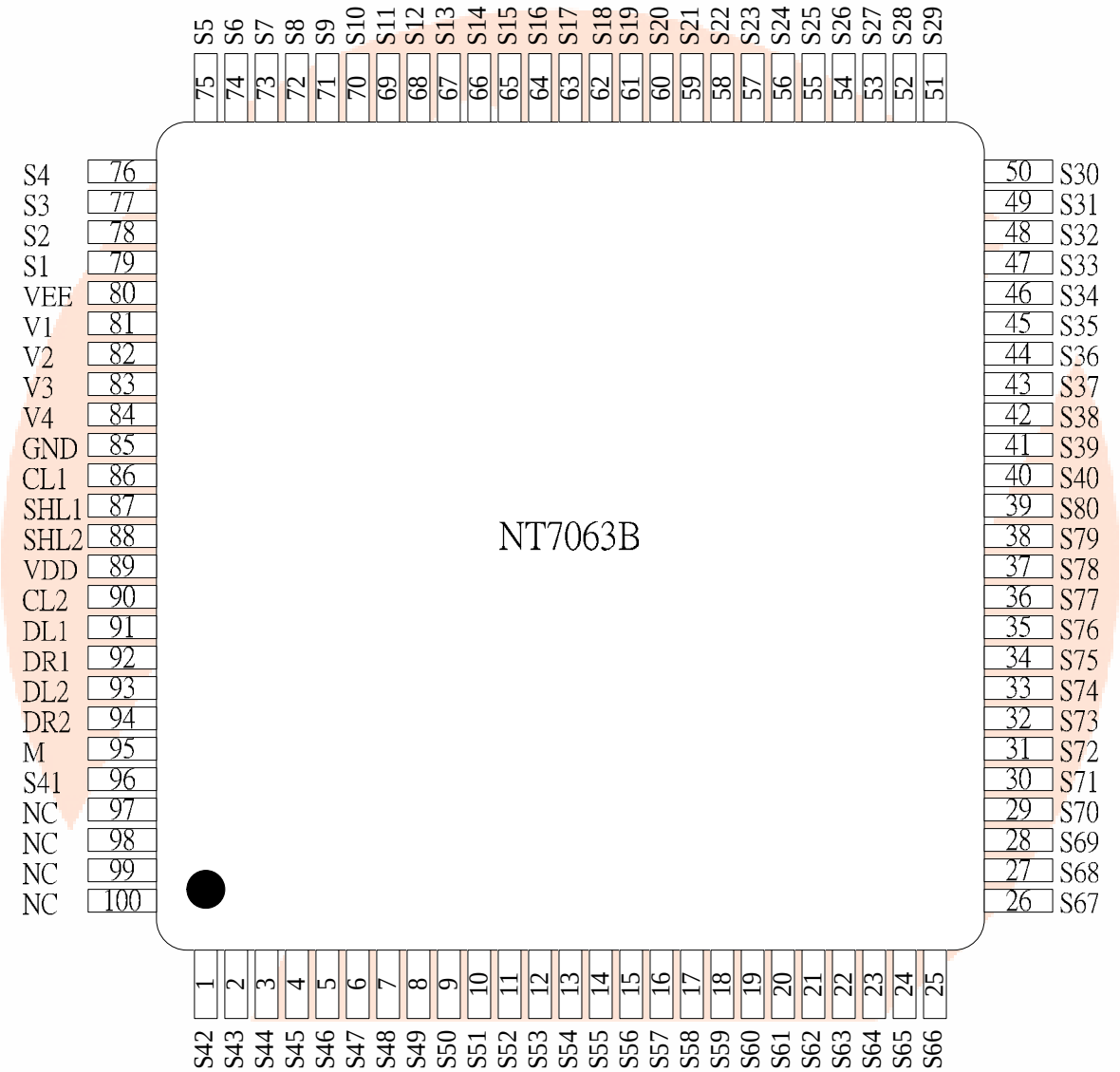
SYMBOLS	MIN.	NOM	MAX.
A	–	–	–
A1	0.10	–	0.50
A2	2.50	–	2.90
b	0.20	0.30	0.40
c	0.10	0.15	0.20
D	24.60	24.80	25.00
D1	19.90	20.00	20.10
e	0.498	0.65	0.802
E	18.60	18.80	19.00
E1	13.90	14.00	14.10
L	1.00	1.20	1.40
L1	–	2.40	–
θ°	0	–	7
y	–	–	0.10

UNIT : mm

NOTES:
1.JEDEC OUTLINE:MO-112 CC-1
2.DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H .
4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION .



Pin Configuration (100 LQFP)



100 LQFP Outline Dimension

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN	NOM	MAX
A			1.60			0.063
A1	0.05		0.15	0.001		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09		0.16	0.004		0.006
e		0.50 BASIC			0.020 BASIC	
D		16.00 BASIC			0.630 BASIC	
D1		14.00 BASIC			0.551 BASIC	
E		16.00 BASIC			0.630 BASIC	
E1		14.00 BASIC			0.551 BASIC	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00 REF.			0.039 REF.	
R1	0.08			0.003		
R	0.08		0.20	0.003		0.008
θ	0	3.5	7	0	3.5	7
θ1	0			0		
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
JEDEC	MS-026 (BED)					

⚠ *NOTES : DIMENSIONS " D1 " AND " E1 " DO NOT INCLUDE MOLD PROTRUSION ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE " D1 AND " E1 " ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD